

TYPES SN54S281, SN74S281 4-BIT PARALLEL BINARY ACCUMULATORS

FEBRUARY 1974 - REVISED DECEMBER 1983

- Full 4-Bit Binary Accumulator in a Single Package
- 15 Arithmetic/Logic-Type Operations:
 - Add
 - Subtract (B-A or A-B)
 - Complement
 - Increment
 - Transfer
 - Plus 10 Other Functions
- Full Shifting Capabilities:
 - Logic Shift (Left or Right)
 - Arithmetic Shift (Left or Right) for Sign Bit Protection
 - Hold
 - Parallel Load
- Expandable to Handle n-Bit Words with Full Carry Look-Ahead
- Logic Mode Operation Provides Seven Boolean Functions of the Two Variables

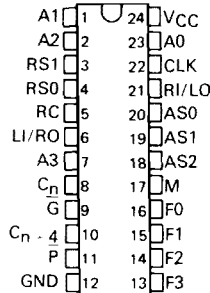
description

These Schottky-clamped four-bit accumulators integrate high-performance versions of an arithmetic logic unit/function generator and a shift/storage matrix on a single monolithic circuit bar. The arithmetic logic unit (ALU) portion, similar to the SN54S181/SN74S181 circuit, incorporates the capability to perform 16 arithmetic/logic-type operations as detailed in Table 1. The accumulator includes an exchange of subtract operands by which either A-B or B-A can be accomplished directly. The ALU is controlled by three function-select inputs (AS0, AS1, AS2) and a mode-control input (M). When the mode-control input is high, the ALU is placed in a logic mode that performs any of seven logic functions on two binary variables as detailed in Table 2. Full carry look-ahead is provided for fast, simultaneous carry generation for the full four binary bits. The carry input (C_n) and propagate and generate outputs (P, G) are implemented for direct use with the SN54S182/SN74S182 look-ahead carry generators. This permits systems to be implemented with the added advantage of full look-ahead across any word length to minimize the accumulator delay times. Once data is loaded into the accumulator, the typical add time with full look-ahead is 29 nanoseconds for 16-bit words.

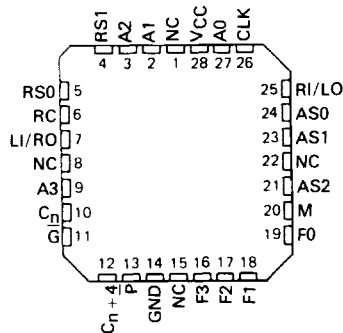
The shift/storage matrix is analogous in its capabilities to the SN54S194/SN74S194 universal bidirectional shift register with the added advantages of multiplexed input/output (I/O) cascading lines that comprehend arithmetic shift functions having a sign bit, such as 2's complements. The matrix can be used to perform either logic or arithmetic shifts in either direction (left or right), parallel load, or hold. Control of the register is accomplished with three inputs: register control (RC) and register selection (RS0, RS1). The cascading input/output lines incorporate three-state outputs multiplexed with an input. The least-significant cascading bit is combined with the A0, F0 circuitry to provide the shift-right input and the shift-left output (RI/LO), and the most significant bit is coupled with the A3, F3 circuitry to provide the shift-left input and the shift-right output (LI/RO).

Series 54S circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74S circuits are characterized for operation from 0°C to 70°C.

SN54S281 ... J OR W PACKAGE
SN74S281 ... DW, J OR N PACKAGE
(TOP VIEW)



SN54S281 ... FK PACKAGE
SN74S281 ... FN PACKAGE
(TOP VIEW)



NC - No internal connection

PRODUCTION DATA
This document contains information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters

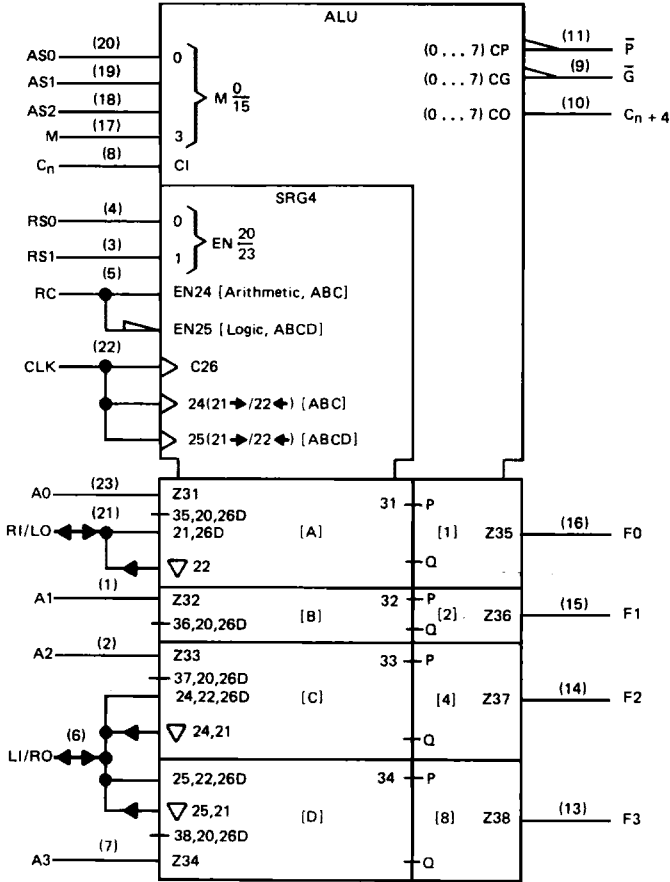


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4-BIT PARALLEL BINARY ACCUMULATORS

logic symbol



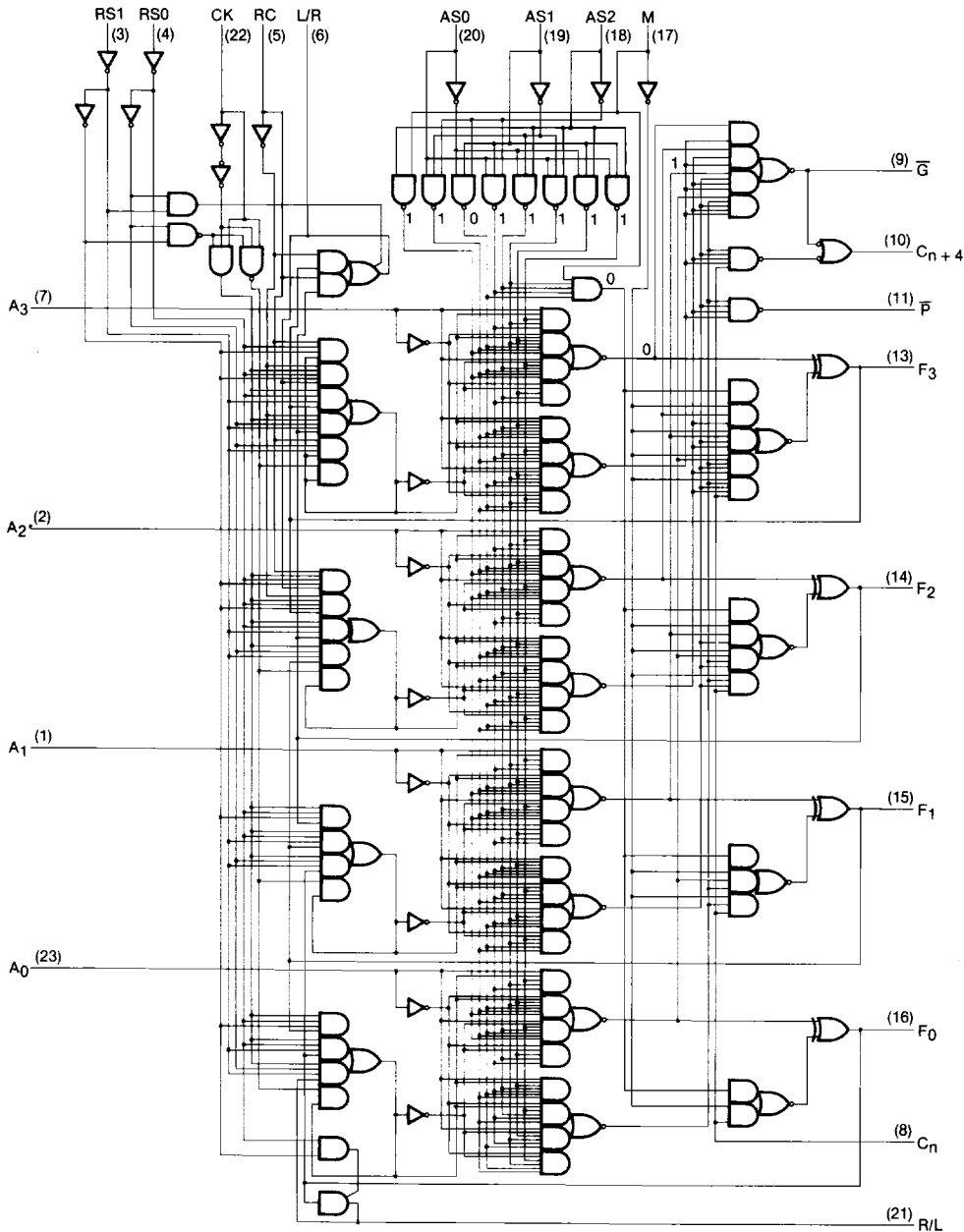
Pin numbers shown on logic notation are for DW, J or N packages.

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logic diagram



TYPES SN54S281, SN74S281

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FUNCTION TABLES

TABLE 1—ARITHMETIC FUNCTIONS
Mode Control (M) = Low

ALU SELECTION			ACTIVE-HIGH DATA			
AS2	AS1	AS0	C _n = H (with carry)		C _n = L (no carry)	
L	L	L	F ₀ = L, F ₁ = F ₂ = F ₃ = H			F _n = H
L	L	H	F = B MINUS A			F = B MINUS A MINUS 1
L	H	L	F = A MINUS B			F = A MINUS B MINUS 1
L	H	H	F = A PLUS B PLUS 1			F = A PLUS B
H	L	L	F = B PLUS 1			F _n = B _n
H	L	H	F = B PLUS 1			F _n = B _n
H	H	L	F = A PLUS 1			F _n = A _n
H	H	H	F = A̅ PLUS 1			F _n = A̅ _n

TABLE 2—LOGIC FUNCTIONS
Mode Control (M) = High
Carry Input (C_n) = X (Irrelevant)

ALU SELECTION			ACTIVE-HIGH DATA FUNCTION			
AS2	AS1	AS0				
L	L	L	F _n = L			
L	X	H	F _n = A _n ⊕ B _n			
L	H	L	F _n = A _n ⊕ B _n			
H	L	L	F _n = A _n B _n			
H	L	H	F _n = A _n + B _n			
H	H	L	F _n = A _n B _n			
H	H	H	F _n = A _n + B _n			

TABLE 3—SHIFT-MODE FUNCTIONS
C_n = M = AS0 = AS1 = L, and AS2 = H (F_n = B_n)

FUNCTION	INPUTS BEFORE †										OUTPUTS AFTER †					
	REGISTER SELECTION		REGISTER CONTROL	INPUT/OUTPUT	SHIFT-MATRIX INPUTS				INPUT/OUTPUT	CLOCK INPUT	INPUT/OUTPUT	SHIFT-MATRIX OUTPUTS (ALU B INPUTS)				INPUT/OUTPUT
	RS0	RS1	INPUT	RI/LO	F0	F1	F2	F3	LI/RO		RI/LO	Q _A	Q _B	Q _C	Q _D	LI/RO
LOAD	L	L	X	Z	f0	f1	f2	f3	Z	↑	Z	f0	f1	f2	f3	Z
LSL	L	H	L	Q _A	Q _A	Q _B	Q _C	Q _D	li	↑	Q _{Bn}	Q _{Bn}	Q _{Cn}	Q _{Dn}	li	li
LSA	L	H	H	Q _A	Q _A	Q _B	Q _C	Q _D	li	↑	Q _{Bn}	Q _{Bn}	Q _{Cn}	li	Q _{D0}	li
RSL	H	L	L	ri	Q _A	Q _B	Q _C	Q _D	Q _D	↑	ri	ri	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
RSA	H	L	H	ri	Q _A	Q _B	Q _C	Q _D	Q _C	↑	ri	ri	Q _{An}	Q _{Bn}	Q _{D0}	Q _{Bn}
HOLD	H	H	X	X	Q _A	Q _B	Q _C	Q _D	X	↑	Z	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Z
	X	X	X	X	Q _A	Q _B	Q _C	Q _D	X	L	RI/LO	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	LI/RO

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

Z = high impedance (output off)

† = transition from low to high level

f0, f1, f2, f3, ri, li = the level of steady-state conditions at F0, F1, F2, F3, RI/LO, or LI/RO respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent transition of the clock

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S281 (see Note 2)	-55°C to 125°C
SN74S281	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. An SN54S281 in the W package operating at free-air temperatures above 110°C requires a heat sink that provides thermal resistance from case to free-air, R_{θCA}, of not more than 20°C/W.

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recommended operating conditions

		SN54S281			SN74S281			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except LI/RO and RI/LO	-1			-1			mA
	LI/RO and RI/LO	-2			-2			
Low-level output current, I_{OL}	Any output except LI/RO and RI/LO	20			20			mA
	LI/RO and RI/LO	10			10			
Clock frequency, f_{clock} (for shifting)		0		50	0		50	MHz
Width of clock pulse, $t_w(\text{clock})$		8			8			ns
Data setup time with respect to clock, t_{SU}		0†			0†			ns
Data hold time with respect to clock, t_H		18†			18†			ns
Operating free-air temperature, T_A (see Note 2)		-55		125	0		70	°C

†The arrow indicates that the rising edge of the clock pulse is used for reference.

NOTE 2: An SN54S281 in the W package operating at free-air temperatures above 110°C requires a heat sink that provides thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 20°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S281			SN74S281			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage		0.8			0.8			V
V_{IK}	Input clamp voltage	Any input except LI/RO and RI/LO $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.2			-1.2			V
V_{OH}	High-level output voltage	Any output except LI/RO and RI/LO $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.5	3.4		2.7	3.4		V
		LI/RO, RI/LO	2.4	3.4		2.4	3.4		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = \text{MAX}$	0.5			0.5			V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
I_{IH}	High-level input current	RS0, RS1	50			50			μA
		M, Clock	150			150			
		LI/RO, RI/LO	200			200			
		AS2	300			300			
		All others	250			250			
I_{IL}	Low-level input current	RS0, RS1, LI/RO	-2			-2			mA
		RI/LO	-3			-3			
		M, Clock	-4			-4			
		AS0, AS1	-6			-6			
		All others	-8			-8			
I_{OS}	Short-circuit output current‡	$V_{CC} = \text{MAX}$	-40	-110	-40	-110	mA		
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ $T_A = 125^\circ\text{C}$ W package only	190						mA
		$V_{CC} = \text{MAX}$ All packages	144	230	144	230			

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 3: When testing input current at the RI/LO or LI/RO terminals, the output under test must be in the high-impedance (off) state.

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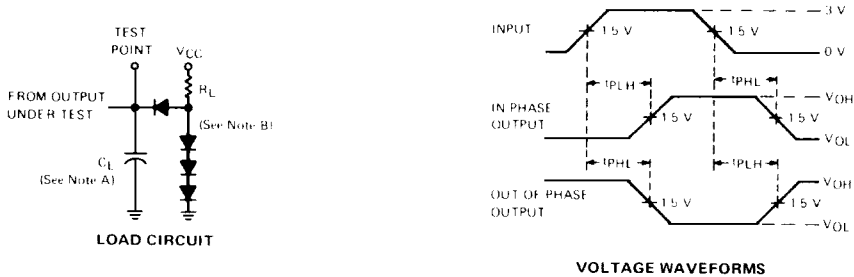
4-BIT PARALLEL BINARY ACCUMULATORS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{ C}$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}	$C_L = 15\text{ pF}$, I/O outputs: $R_L = 560\ \Omega$, Other outputs: $R_L = 280\ \Omega$, See Figure 1	10	20	ns	
t_{PHL}				10	20		
t_{PLH}	Any A	C_{n+4}		18	30	ns	
t_{PHL}				18	30		
t_{PLH}	C_n	Any F		10	20	ns	
t_{PHL}				10	20		
t_{PLH}	Any A	\bar{G}		14	24	ns	
t_{PHL}				14	24		
t_{PLH}	Any A	\bar{P}		12	20	ns	
t_{PHL}				12	20		
t_{PLH}	A_i	F_i		20	35	ns	
t_{PHL}				20	35		
t_{PLH}	A_0	RI/LO		30	45	ns	
t_{PHL}				30	45		
t_{PLH}	A_3	LI/RO	30	45	ns		
t_{PHL}			30	45			
t_{PLH}	F_0	RI/LO	7	11	ns		
t_{PHL}			7	11			
t_{PLH}	F_3	LI/RO	7	11	ns		
t_{PHL}			7	11			
t_{PLH}	Any AS	Any F or C_{n+4}	28	45	ns		
t_{PHL}			28	45			
t_{PLH}	Any AS	\bar{P} or \bar{G}	20	33	ns		
t_{PHL}			20	33			
t_{PLH}	Clock	Any F	30	45	ns		
t_{PHL}			30	45			
t_{PLH}	Clock	RI/LO or LI/RO	35	55	ns		
t_{PHL}			35	55			

¹ t_{PLH} Propagation delay time, low to high level output
 t_{PHL} Propagation delay time, high to low level output

PARAMETER MEASUREMENT INFORMATION

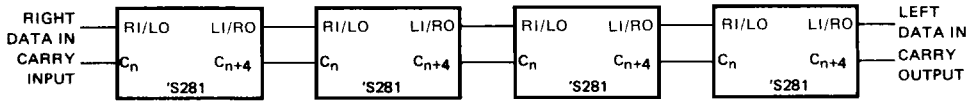


NOTES: A. Input pulse is supplied by a generator having the following characteristics: $t_r = 2.5\text{ ns}$, $t_f = 2.5\text{ ns}$, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.

FIGURE 1

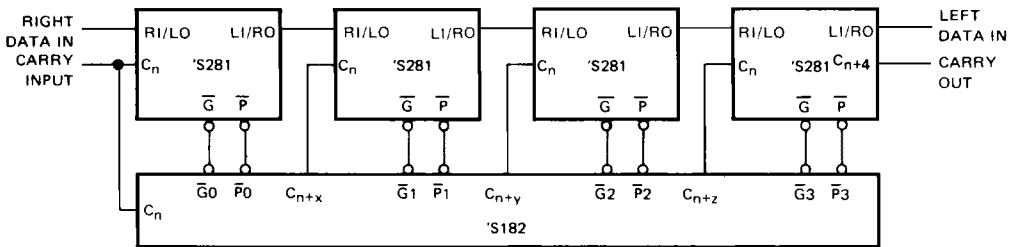
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TYPICAL APPLICATION DATA



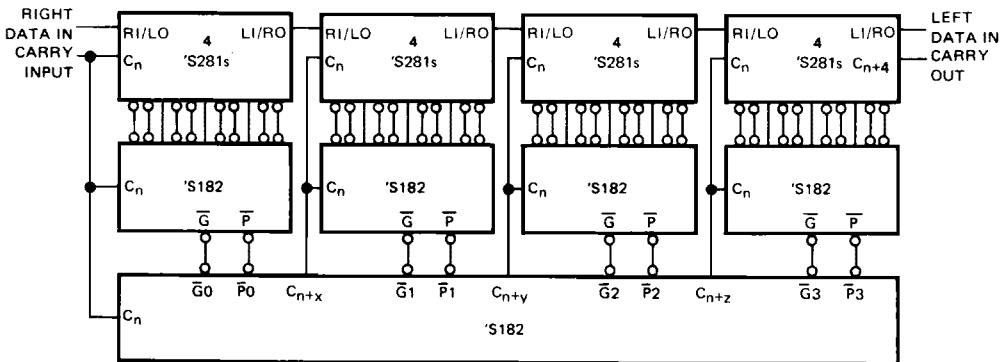
ENTER AND STORE TIME: 38 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 44 ns typical

FIGURE A—16-BIT BINARY ACCUMULATOR USING FOUR SN54S281/SN74S281 CIRCUITS IN RIPPLE-CARRY MODE



ENTER AND STORE TIME: 37 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 29 ns typical

FIGURE B—16-BIT BINARY ACCUMULATOR USING FOUR SN54S281/SN74S281 CIRCUITS AND ONE SN54S182/SN74S182 IN FULL LOOK-AHEAD CARRY MODE



ENTER AND STORE TIME: 42 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 34 ns typical

FIGURE C—64-BIT BINARY ACCUMULATOR USING 16 SN54S281/SN74S281 CIRCUITS AND FIVE SN54S182/SN74S182 CIRCUITS FOR FULL CARRY LOOK-AHEAD

A inputs and F outputs of 'S281 are not shown.

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