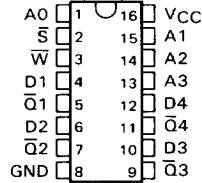


**SN54S189B, SN54S289B, SN74S189B, SN74S289B**  
**64-BIT HIGH-PERFORMANCE**  
**RANDOM-ACCESS MEMORIES**  
 SEPTEMBER 1976—REVISED FEBRUARY 1984

**STATIC RANDOM-ACCESS MEMORIES**

- Fully Decoded RAMs Organized as 16 Words of Four Bits Each
- Schottky-Clamped for High Speed:  
 Read Cycle Time . . . 25 ns Typical  
 Write Cycle Time . . . 25 ns Typical
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I<sup>2</sup>L Circuits
- Chip-Select Input Simplifies External Decoding

SN54S189B, SN54S289B . . . J OR W PACKAGE  
 SN74S189B, SN74S289B . . . J OR N PACKAGE  
 (TOP VIEW)



**description**

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four bits each. They are fully decoded and feature a chip-select input to simplify decoding required to achieve expanded system organization. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of -0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor. The chip-select circuitry is implemented with minimal delay times to compensate for added system decoding.

**write cycle**

The information applied at the data input is written into the selected location when the chip-select input and the write-enable input are low. While the write-enable input is low, the 'S189B output is in the high-impedance state and the 'S289B output is off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

**read cycle**

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the 'S189B output will be in the high-impedance state and the 'S289B output will be off.

FUNCTION TABLE

FUNCTION	INPUTS		'S189B OUTPUT	'S289B OUTPUT
	CHIP SELECT	WRITE ENABLE		
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

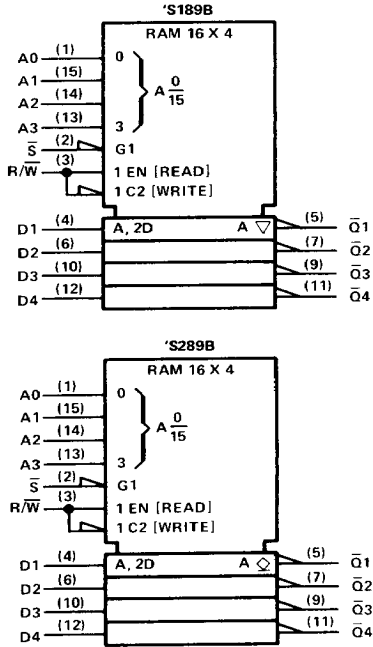
H = high level, L = low level, X = irrelevant

**5**  
**RAMS**

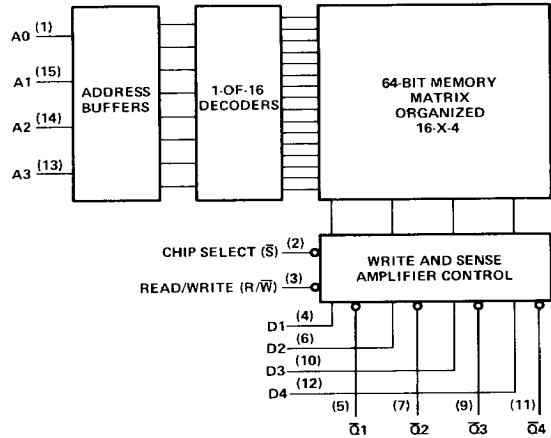
# SN54S189B, SN54S289B, SN74S189B, SN74S289B

## 64-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

### logic symbols



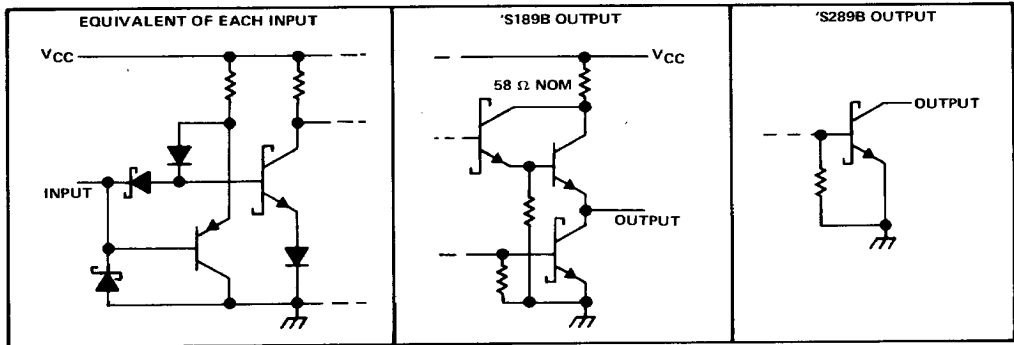
### functional block diagram



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RAMS

### schematics of inputs and outputs



**SN54S189B, SN54S289B, SN74S189B, SN74S289B**  
**64-BIT HIGH-PERFORMANCE**  
**RANDOM-ACCESS MEMORIES**

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) . . . . .	7 V
Input voltage . . . . .	5.5 V
Off-State output voltage . . . . .	5.5 V
Operating free-air temperature range: SN54S' Circuits . . . . .	-55°C to 125°C
SN74S' Circuits . . . . .	0°C to 70°C
Storage temperature range . . . . .	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

		SN54S'			SN74S'			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V		
High-level output voltage, $V_{OH}$		'S289B			5.5			V		
High-level output current, $I_{OH}$		'S189B			-6.5			mA		
Low-level output current, $I_{OL}$					16			mA		
Width of write pulse (write enable low), $t_{w(wr)}$		25			25			ns		
Setup time	Address before write pulse, $t_{su(da)}$	0†			0‡			ns		
	Data before end of write pulse, $t_{su(da)}$	25†			25†					
	Chip-select before end of write pulse, $t_{su(S)}$	25†			25†					
Hold time	Address after write pulse, $t_h(ad)$	3†			0†			ns		
	Data after write pulse, $t_h(da)$	0†			0†					
	Chip-select after write pulse, $t_h(S)$	0†			0†					
Operating free-air temperature, $T_A$		-55			125			0	70	°C

†‡The arrow indicates the transition of the write-enable input used for reference: † for the low-to-high transition, ‡ for the high-to-low transition.



**SN54S189B, SN54S289B, SN74S189B, SN74S289B**  
**64-BIT HIGH-PERFORMANCE**  
**RANDOM-ACCESS MEMORIES**

**electrical characteristics over recommended operating free-air temperature range**  
**(unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>†</sup>	'S189B			'S289B			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage					0.8			V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA				-1.2			V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX	SN54S <sup>§</sup> 2.4 3.4						V
I <sub>OH</sub> High-level output current	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V	V <sub>O</sub> = 2.4 V			40			μA
		V <sub>O</sub> = 5.5 V			100			μA
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA	0.35 0.5			0.35 0.5			V
I <sub>OZH</sub> Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, V <sub>OH</sub> = 2.4 V	50						μA
I <sub>OZL</sub> Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, V <sub>OL</sub> = 0.4 V	-50						μA
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1			1			mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	25			25			μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V	-250			-250			μA
I <sub>OS</sub> Short-circuit output current <sup>§</sup>	V <sub>CC</sub> = MAX	-30 -100						mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 2	75 110			75 105			mA

NOTE 2: I<sub>CC</sub> is measured with the read/write and chip-select inputs grounded. All other inputs at 4.5 V, and the outputs open.

**'S189B switching characteristics over recommended operating ranges of T<sub>A</sub> and V<sub>CC</sub>**  
**(unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54S189B		SN74S189B		UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	
t <sub>a(ad)</sub> Access time from address	C <sub>L</sub> = 30 pF, See Note 3	25 50		25 35		ns
t <sub>a(S)</sub> Access time from chip select (enable time)		18 25		18 22		ns
t <sub>SR</sub> Sense recovery time		22 40		22 35		ns
t <sub>PXZ</sub> Disable time from high or low level	From $\bar{S}$	12 25		12 17		ns
	From $\bar{W}$	12 30		12 25		

**'S289B switching characteristics over recommended operating ranges of T<sub>A</sub> and V<sub>CC</sub>**  
**(unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54S289B		SN74S289B		UNIT	
		MIN	TYP <sup>‡</sup>	MAX	MIN		TYP <sup>‡</sup>
t <sub>a(ad)</sub> Access time from address	C <sub>L</sub> = 30 pF, R <sub>L1</sub> = 300 Ω, R <sub>L2</sub> = 600 Ω, See Note 3	25 50		25 35		ns	
t <sub>a(S)</sub> Access time from chip-select (enable time)		18 25		18 22		ns	
t <sub>SR</sub> Sense recovery time		22 40		22 35		ns	
t <sub>PLH</sub> Propagation delay time, low-to-high-level output (disable time)		From $\bar{S}$	12 25		12 17		ns
		From $\bar{W}$	12 30		12 25		

<sup>†</sup>For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°.

<sup>§</sup>Duration of the short circuit should not exceed one second.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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