

74LVQ74

Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The LVQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

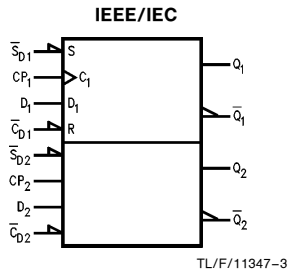
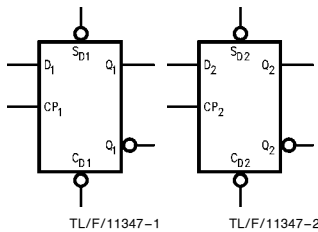
Asynchronous Inputs:

- LOW input to \bar{S}_D (Set) sets Q to HIGH level
- LOW input to \bar{C}_D (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

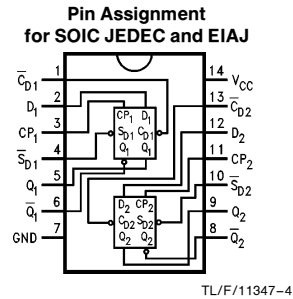
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75 Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

Logic Symbols



Connection Diagram



Pin Names	Description
D ₁ , D ₂	Data Inputs
CP ₁ , CP ₂	Clock Pulse Inputs
\bar{C}_D1 , \bar{C}_D2	Direct Clear Inputs
\bar{S}_D1 , \bar{S}_D2	Direct Set Inputs
Q ₁ , \bar{Q}_1 , Q ₂ , \bar{Q}_2	Outputs

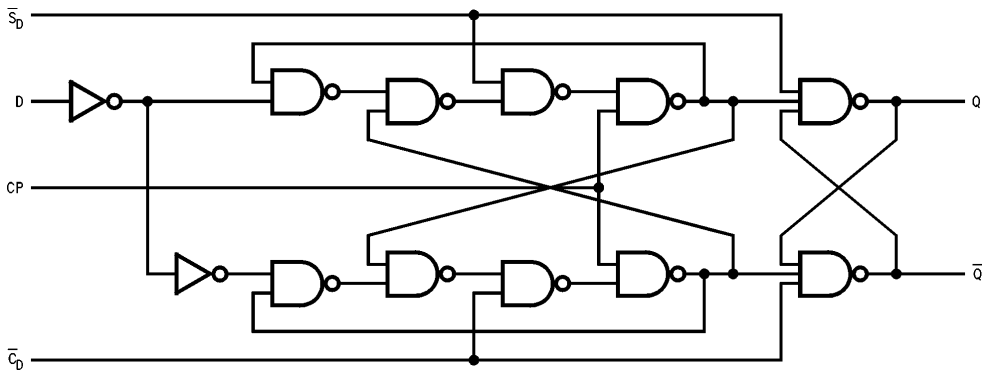
	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ74SC 74LVQ74SCX	74LVQ74SJ 74LVQ74SJX
See NS Package Number	M14A	M14D

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S_D}$	$\overline{C_D}$	CP	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Clock Transition
 ↘ = LOW-to-HIGH Clock Transition
 $Q_0(\overline{Q_0})$ = Previous Q(\overline{Q}) before LOW-to-HIGH Transition of Clock

Logic Diagram



TL/F/11347-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	-20 mA
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	-20 mA
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	± 200 mA
Storage Temperature (T_{STG})	-65°C to +150°C
DC Latch-Up Source or Sink Current	± 100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
LVQ	
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
74LVQ	
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ74		74LVQ74		Units	Conditions
			$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		3.0		2.58	2.48	V	* $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$	
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		3.0		0.36	0.44	V	* $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$	
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	± 1.0	μA	$V_I = V_{CC}, \text{GND}$	

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	74LVQ74		74LVQ74		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	3.6			36	mA	V _{OLD} = 0.8V Max (Note 1)	
I _{OHD}		3.6			-25	mA	V _{OHD} = 2.0V Min (Note 1)	
I _{CC}	Maximum Quiescent Supply Current	3.6		2.0	20.0	μA	V _{IN} = V _{CC} or GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.2	0.8		V	(Notes 2 and 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.2	-0.8		V	(Notes 2 and 3)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Notes 2 and 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2 and 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	74LVQ74			74LVQ74		Units
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	2.7 3.3 ± 0.3	50 100	100 125	16.9 12.0	40 95	MHz	
t _{PLH}	Propagation Delay C _{Dn} or S _{Dn} to Q _n	2.7 3.3 ± 0.3	3.5 3.5	9.6 8.0	16.9 12.0	3.5 2.5	19.0 13.0	ns
t _{PHL}	Propagation Delay C _{Dn} or S _{Dn} to Q _n	2.7 3.3 ± 0.3	4.0 4.0	12.6 10.5	16.9 12.0	3.5 3.5	19.0 13.5	ns
t _{PLH}	Propagation Delay CP _n to Q _n or Q _n	2.7 3.3 ± 0.3	4.5 4.5	9.6 8.0	19.0 13.5	4.0 4.0	23.0 16.0	ns
t _{PHL}	Propagation Delay CP _n to Q _n or Q _n	2.7 3.3 ± 0.3	3.5 3.5	9.6 8.0	19.7 14.0	3.5 3.5	21.0 14.5	ns
t _{OSSL} t _{OSLH}	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSSL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V _{CC} (V)	74LVQ74		74LVQ74	Units
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum		
t _s	Set-up Time, HIGH or LOW	2.7 3.3 ± 0.3	1.8 1.5	5.0 4.0	6.5 4.5	ns
t _H	Hold Time, HIGH or LOW D _n to CP _n	2.7 3.3 ± 0.3	-2.4 -2.0	0.5 0.5	0.5 0.5	ns
t _W	Pulse Width	2.7 3.3 ± 0.3	3.6 3.0	7.0 5.5	10.0 7.0	ns
t _{rec}	Recovery Time	2.7 3.3 ± 0.3	-3.0 -2.5	0 0	0 0	ns

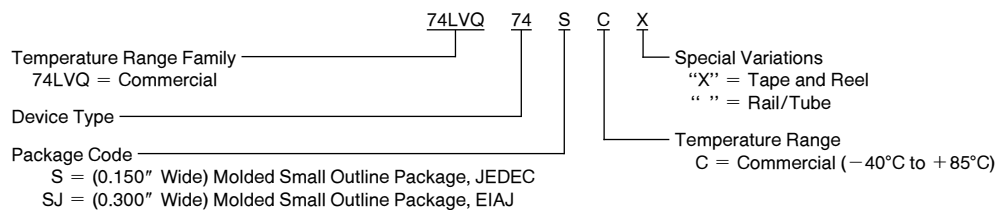
Capacitance

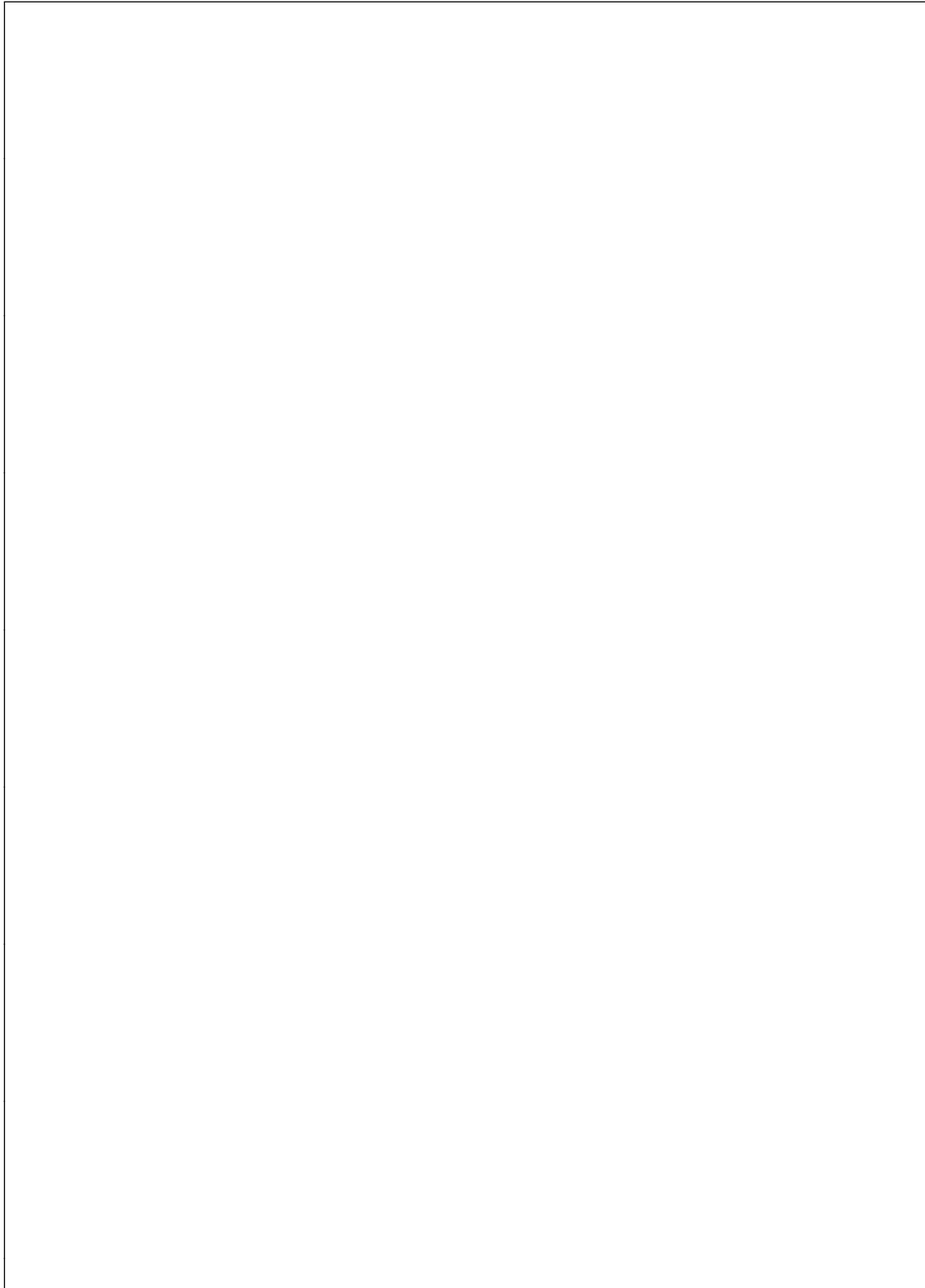
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	25	pF	V _{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

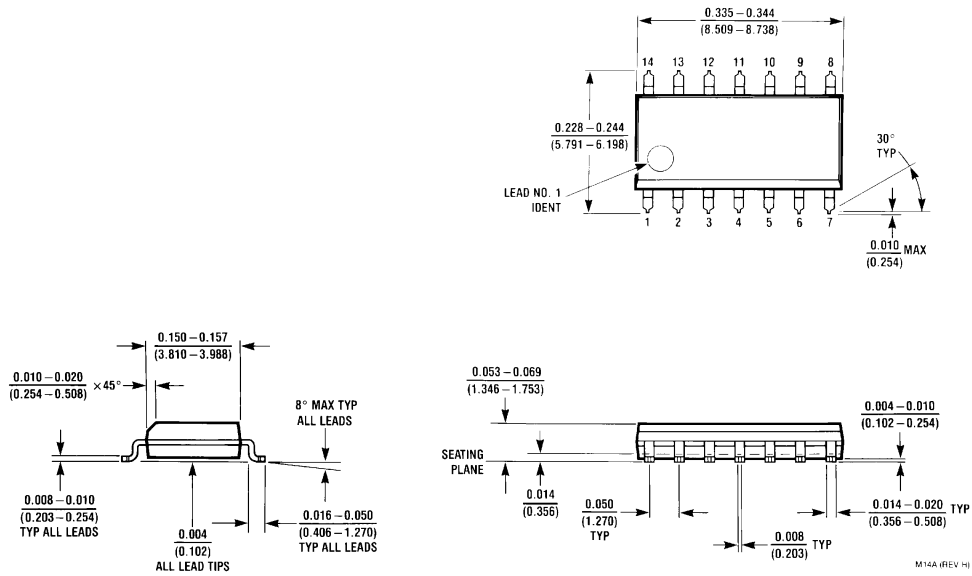
74LVQ74 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:





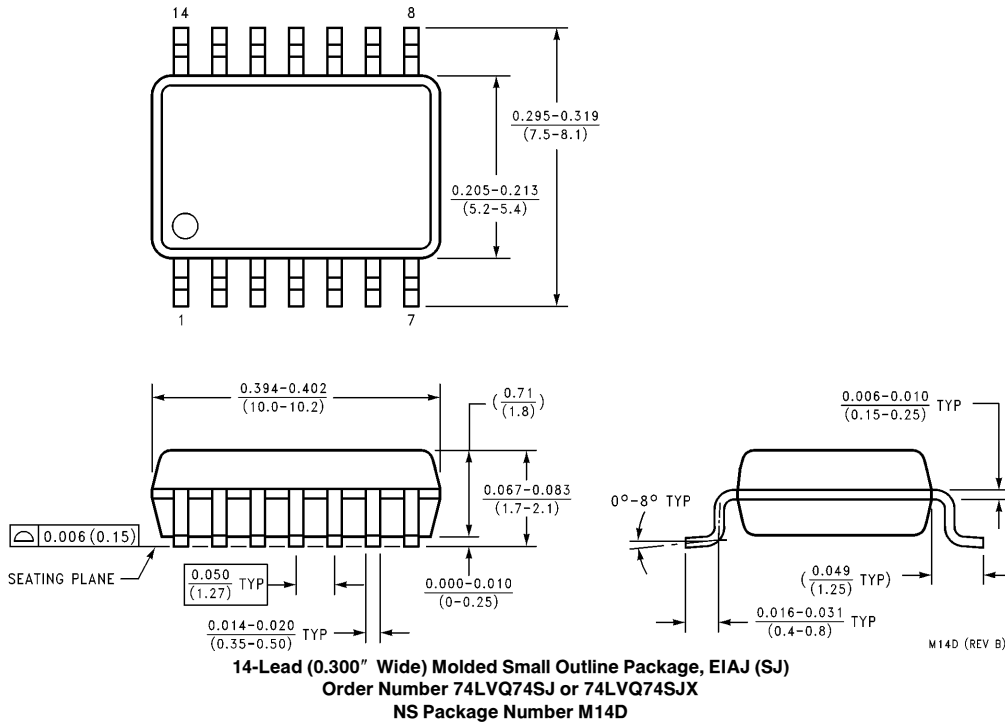
Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead (0.150" Wide) Molded Small Outline Integrated Circuit, JEDEC (SC)
Order Number 74LVQ74SC or 74LVQ74SCX
NS Package Number M14A

M14A (REV H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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