Low-Voltage Quiet CMOS Octal Transceiver/Registered Transceiver

(3-State, Non-Inverting)

MC74LVQ646

LVQ

LOW–VOLTAGE CMOS OCTAL TRANSCEIVER/ REGISTERED TRANSCEIVER

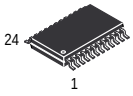
The MC74LVQ646 is a high performance, non–inverting octal transceiver/registered transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. The MC74LVQ646 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW–to–HIGH logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBA, SAB) can multiplex stored and real–time (transparent mode) data. The direction control (DIR) determines which bus will receive data when the enable $\overline{OE}$ is active LOW. In the isolation mode ($\overline{OE}$ HIGH), A data may be stored in the B register or B data may be stored in the A register. Only one of the two buses, A or B, may be driven at one time.

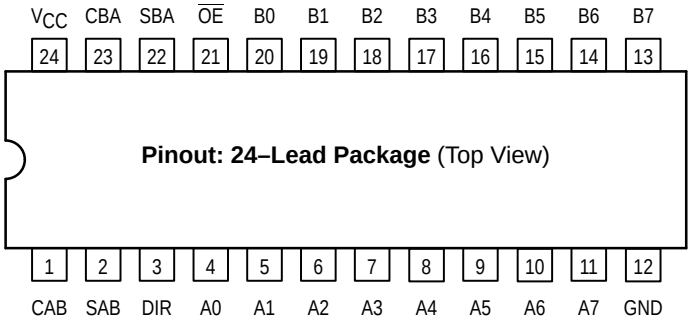
- Designed for 2.7 to 3.6V V_{CC} Operation – Ideal for Low Power/Low Noise Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Guaranteed Skew Specifications
- Guaranteed Incident Wave Switching into 75Ω
- Low Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V

DW SUFFIX
PLASTIC SOIC
CASE 751E–04

SD SUFFIX
PLASTIC SSOP
CASE 940D–03



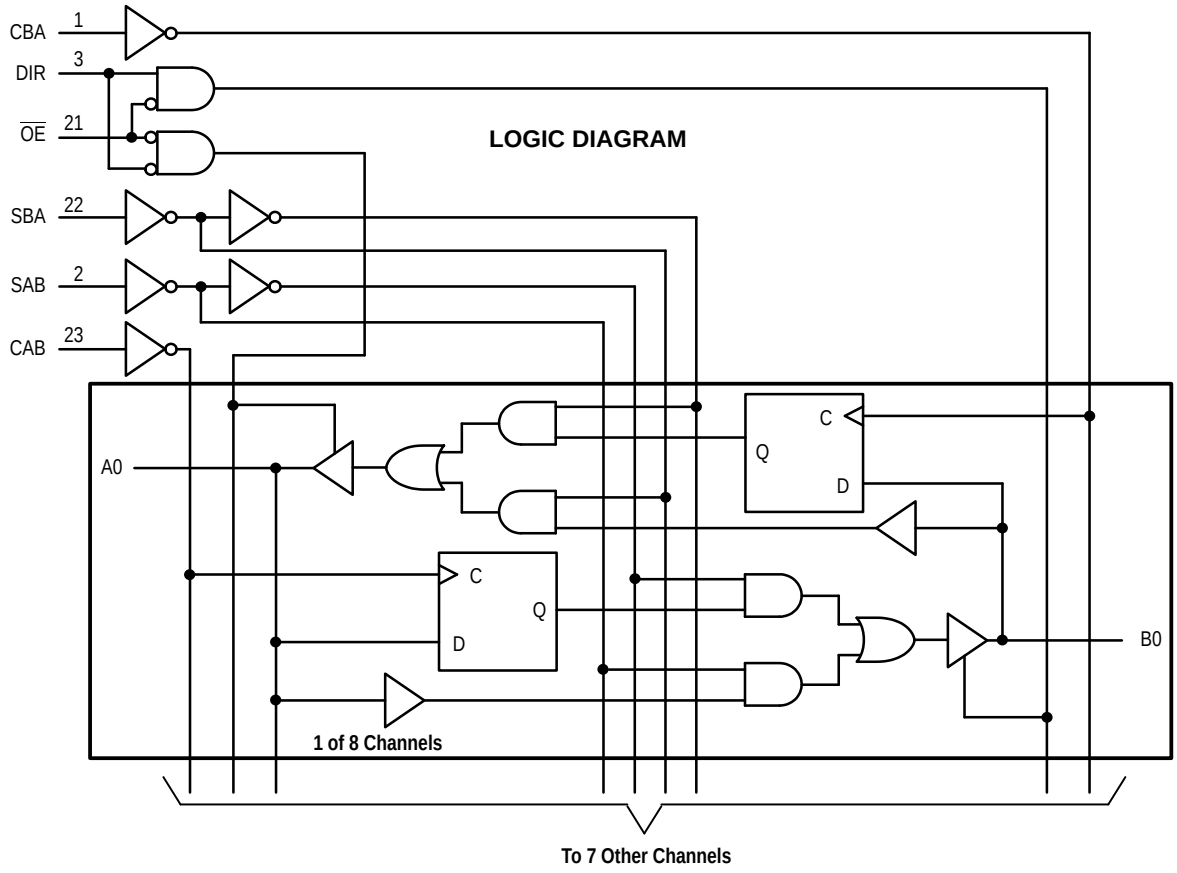
DT SUFFIX
PLASTIC TSSOP
CASE 948H–01



PIN NAMES

Pins	Function
A0–A7	Side A Inputs/Outputs
B0–B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Select Control Inputs
DIR, $\overline{OE}$	Output Enable Inputs

MOTOROLA



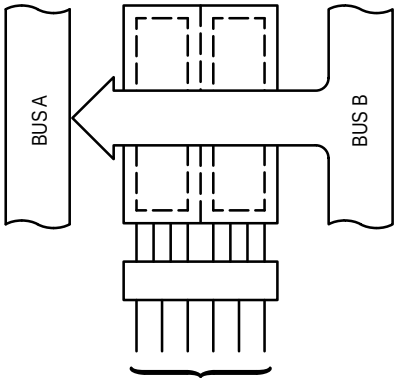
FUNCTION TABLE

Inputs						Storage Registers		Data Ports		Operating Mode
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	QA	QB	An	Bn	Operating Mode
H	X							**Input**	**Input**	
		↥	↥	X	X	NC	NC	X	X	Isolation, Hold Storage
		↑	↑	X	X	L H X X	X X L H	L H X X	X X L H	Store A and/or B Data
L	H							**Input**	**Output**	
		↥	X*	L	X	NC NC	NC NC	L H	L H	Real Time A Data to B Bus
				H	X	NC	NC	X	QA	Stored A Data to B Bus
		↑	X*	L	X	L H	NC NC	L H	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	NC NC	L H	QA QA	Stored A Data to B Bus; Store A Data
L	L							**Output**	**Input**	
		X*	↥	X	L	NC NC	NC NC	L H	L H	Real Time B Data to A Bus
				X	H	NC	NC	QB	X	Stored B Data to A Bus
		X*	↑	X	L	NC NC	L H	L H	L H	Real Time B Data to A Bus; Store B Data
				X	H	NC NC	L H	QB QB	L H	Stored B Data to A Bus; Store B Data

H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = Low–to–High Clock Transition; ↥ = NOT Low–to–High Clock Transition; NC = No Change; * = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I_{CC} reasons, Do Not Float Inputs.

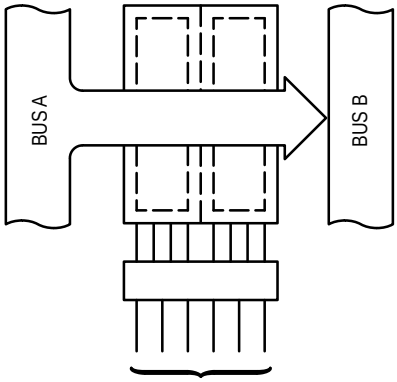
BUS APPLICATIONS

Real Time Transfer – Bus B to Bus A



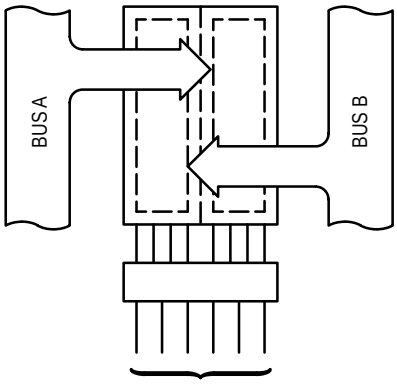
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

Real Time Transfer – Bus A to Bus B



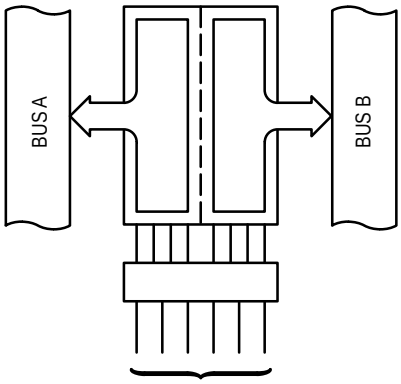
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

Store Data from Bus A, Bus B or Busses A and B



$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer Storage Data to Bus A or Bus B



$\overline{OE}$	DIR	CAB	CBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le V_{CC} + 0.5V$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$	Output in HIGH or LOW State	V
I_{IK}	DC Input Diode Current	–20	$V_I = -0.5V$	mA
		+20	$V_I = V_{CC} + 0.5V$	mA
I_{OK}	DC Output Diode Current	–20	$V_O = -0.5V$	mA
		+20	$V_I = V_{CC} + 0.5V$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current	±400		mA
I_{GND}	DC Ground Current	±400		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.0	3.3	3.6	V
V_I	Input Voltage	0		V_{CC}	V
V_O	Output Voltage	0		V_{CC}	V
T_A	Operating Free–Air Temperature	–40		+85	°C
$\Delta V/\Delta t$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0		125	mV/ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$, V_O = 0.1V or V_{CC} – 0.1V	2.0		V
V_{IL}	LOW Level Input Voltage (Note 1)	$2.7V \le V_{CC} \le 3.6V$, V_O = 0.1V or V_{CC} – 0.1V		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OH} = –50µA	V_{CC} – 0.1		V
		V_{CC} = 2.7V; I_{OH} = –12mA	2.2		
		V_{CC} = 3.0V; I_{OH} = –12mA	2.48		
V_{OL}	LOW Level Output Voltage	$2.7V \le V_{CC} \le 3.6V$; I_{OL} = 50µA		0.1	V
		$2.7V \le V_{CC} \le 3.6V$; I_{OL}= 12mA		0.4	
I_I	Input Leakage Current	$2.7V \le V_{CC} \le 3.6V$; $V_I = V_{CC}$, GND		±1.0	µA
I_{OZT}	Maximum I/O Leakage Current	$V_I(\overline{OE}) = V_{IL}$, V_{IH}; V_I, $V_O = V_{CC}$, GND		±3	µA
I_{OLD}	Minimum Dynamic Output Current (Note 2)	V_{CC} = 3.6V; V_{OLD} = 0.8V Max		36	mA
I_{OHD}		V_{CC} = 3.6V; V_{OHD} = 2.0V Min		–25	mA
I_{CC}	Quiescent Supply Current	$2.7V \le V_{CC} \le 3.6V$; $V_I = V_{CC}$, GND		10	µA

1. These values of V_I are used to test DC electrical characteristics only. Functional test should use $V_{IH} \ge 2.4V$, $V_{IL} \le 0.5V$.
2. Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed. Maximum test duration is 2ms, one output loaded at a time.

DYNAMIC SWITCHING CHARACTERISTICS (V_{CC} = 3.3V)

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 1)	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		0.6	1.0	V
V_{OLV}	Dynamic LOW Valley Voltage (Note 1)	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V		–0.5	–1.0	V
V_{IHD}	High Level Dynamic Input Voltage (Note 2)	Input–Under–Test Switching 0V to Threshold, f=1MHz		1.5	2.0	V
V_{ILD}	Low Level Dynamic Input Voltage (Note 2)	Input–Under–Test Switching 3.3V to Threshold, f=1MHz		1.5	0.8	V

1. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW. The remaining output is measured in the LOW state.
2. Number of data inputs is defined as “n” switching, “n–1” inputs switching 0V to 3.3V.

AC CHARACTERISTICS[1] ($t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω)

Symbol	Parameter	Limits									Unit
		T_A = +25°C						T_A = –40°C to +85°C			
		V_{CC} = 3.0V to 3.6V			V_{CC} = 2.7V			V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V	
		Min	Typ	Max	Min	Typ	Max	Min	Max	Max	
f_{max}	Clock Pulse Frequency	150						150			MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	1.5 1.5	12.5 10.0	15.0 13.0	1.5 1.5	14.0 12.0	18.0 15.0	1.5 1.5	17.0 14.5	20.0 17.0	ns
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1.5 1.5	9.5 8.0	12.0 11.0	1.5 1.5	11.0 9.5	13.5 12.5	1.5 1.5	13.5 12.0	14.5 14.0	ns
t_{PLH} t_{PHL}	Propagation Delay Select to Output	1.5 1.5	9.5 8.5	12.0 11.0	1.5 1.5	11.0 10.0	13.0 12.5	1.5 1.5	13.0 12.5	14.5 14.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to An, Bn	1.5 1.5	8.0 9.0	10.5 11.0	1.5 1.5	9.5 10.0	12.0 12.5	1.5 1.5	11.0 12.0	13.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to An, Bn	1.5 1.5	9.0 8.5	11.0 10.5	1.5 1.5	10.5 9.5	12.5 12.5	1.5 1.5	12.0 12.0	14.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to An, Bn	1.5 1.5	9.0 10.0	12.0 12.0	1.5 1.5	12.0 11.0	14.0 14.0	1.5 1.5	13.0 12.5	16.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to An, Bn	1.5 1.5	9.0 10.0	11.0 12.5	1.5 1.5	10.0 13.0	13.0 15.5	1.5 1.5	12.0 14.0	15.0 18.0	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 2)		1.0 1.0	1.5 1.5			1.0 1.0	1.5 1.5	1.5 1.5		ns

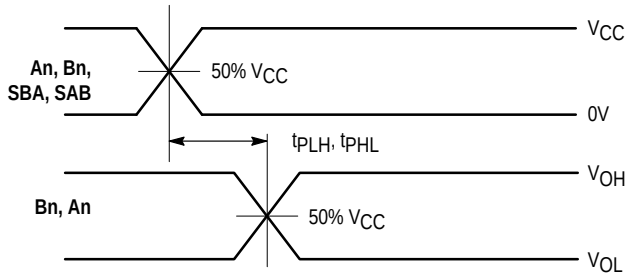
1. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

AC OPERATING REQUIREMENTS ($t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω)

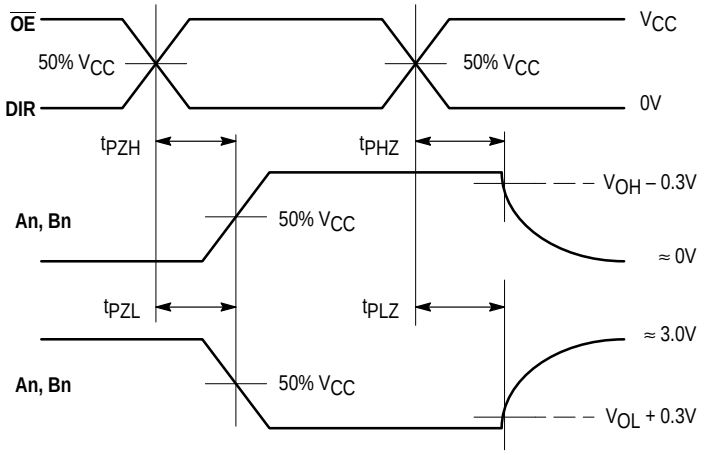
Symbol	Parameter	Limits				Unit
		T_A = +25°C		T_A = –40°C to +85°C		
		V_{CC} = 3.0V to 3.6V	V_{CC} = 2.7V	V_{CC} = 3.0V to 3.6V	V_{CC} = 2.7V	
		Min	Min	Min	Min	
t_s	Setup TIme, HIGH or LOW Dn to LE	2.5	4.0	2.5	4.5	ns
t_h	Hold TIme, HIGH or LOW Dn to LE	1.5	1.5	1.5	1.5	ns
t_w	LE Pulse Width, HIGH	3.3	5.0	3.3	6.0	ns

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{PD}	Power Dissipation Capacitance	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	50	pF
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	4.5	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	15	pF

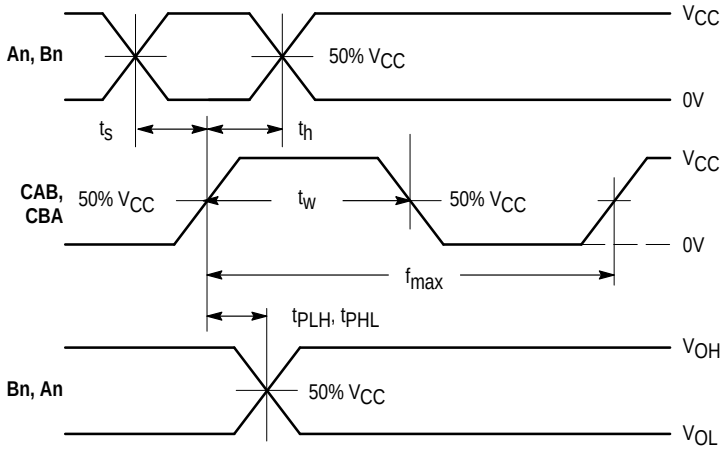


WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns



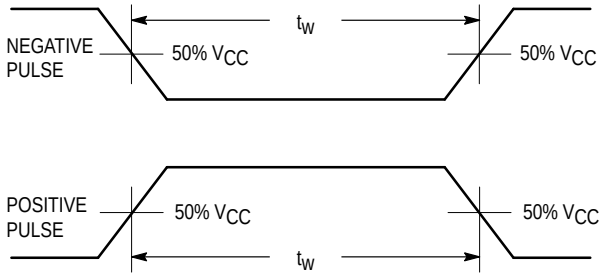
WAVEFORM 2 – $\overline{OE}$/DIR to An/Bn OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns

Figure 1. AC Waveforms



WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES

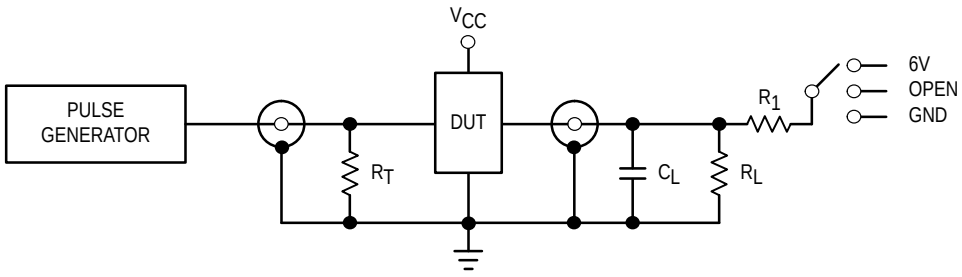
$t_R = t_F$ = 2.5ns, 10% to 90%; f = 1MHz; t_W = 500ns except when noted



WAVEFORM 4 – INPUT PULSE DEFINITION

$t_R = t_F$ = 2.5ns, 10% to 90% of 0V to V_{CC}

Figure 2. AC Waveforms



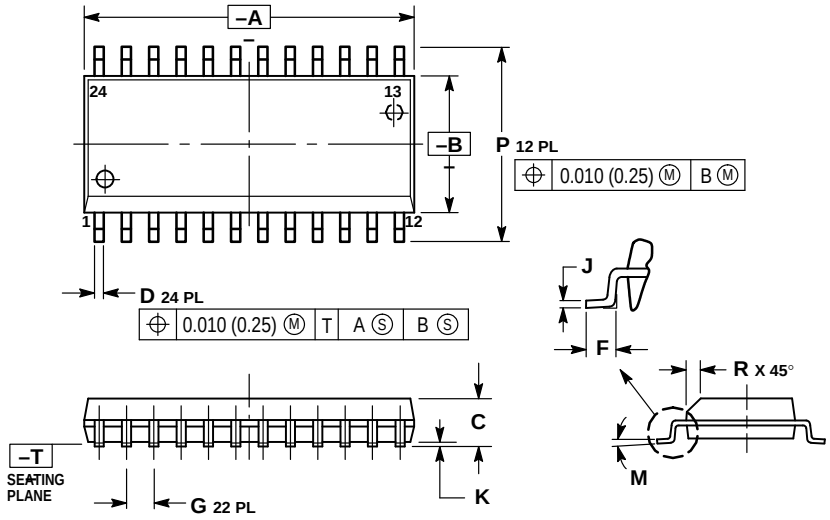
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit

OUTLINE DIMENSIONS

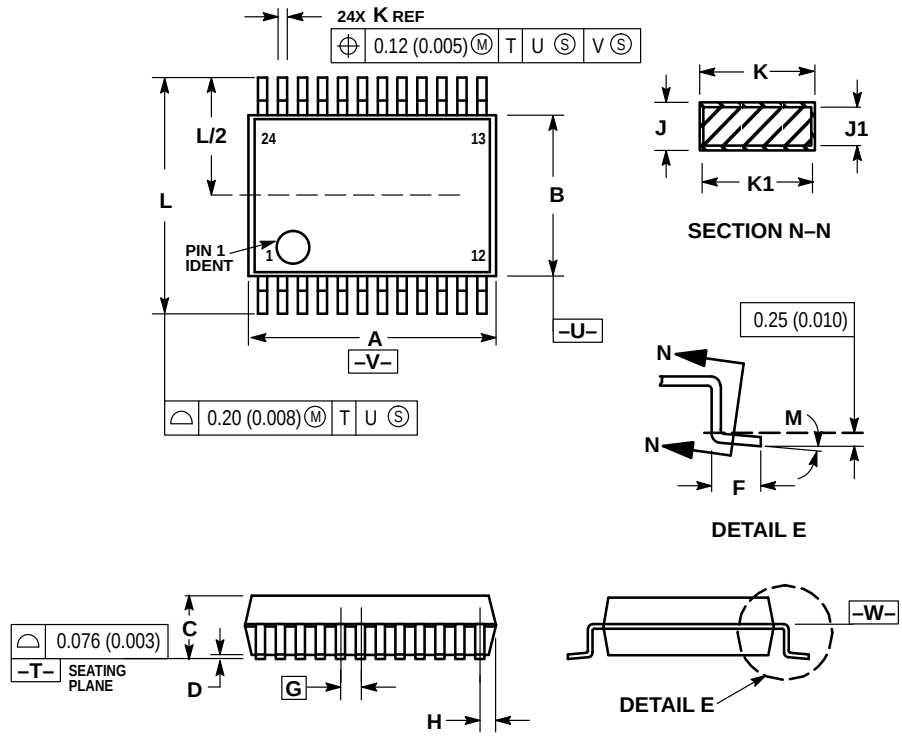
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940D–03
ISSUE B

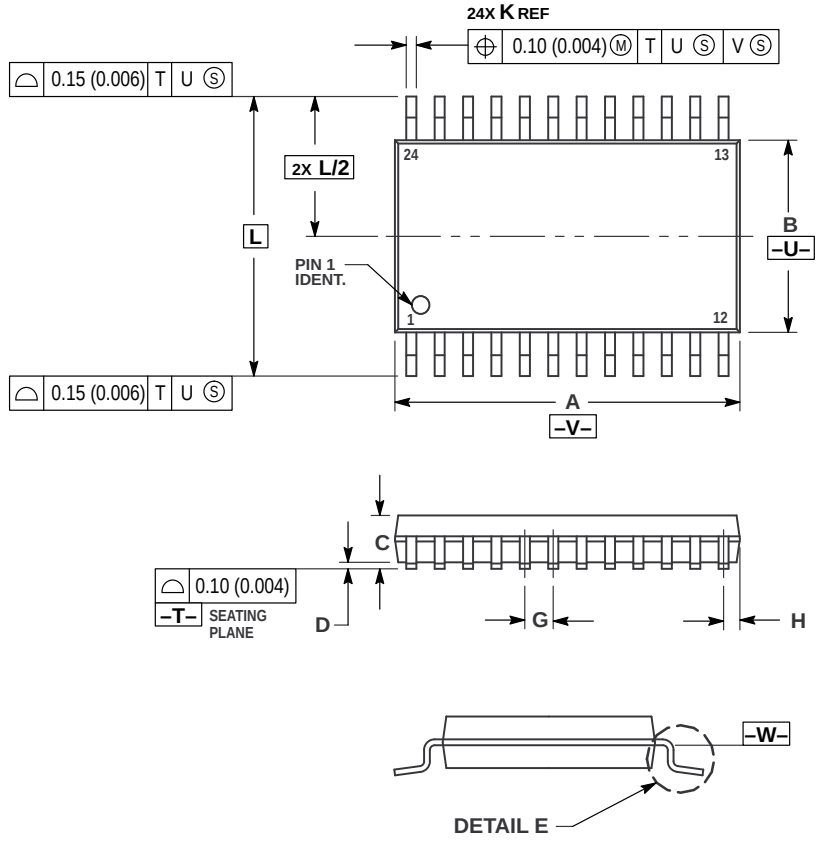


NOTES:
4 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5 CONTROLLING DIMENSION: MILLIMETER.
6 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
7 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
8 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
9 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
10 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 ◦	8 ◦	0◦	8◦

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948H–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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