

74LVQ573

Low Voltage Octal Latch with TRI-STATE® Outputs

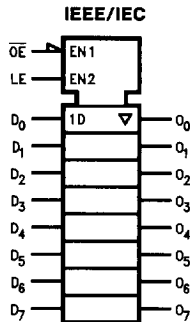
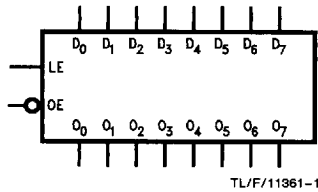
General Description

The LVQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs. The LVQ573 is functionally identical to the LVQ373 but with inputs and outputs on opposite sides of the package.

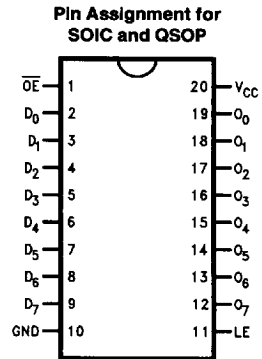
Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75 Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Logic Symbols



Connection Diagram



Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
\overline{OE}	TRI-STATE Output Enable Input
Q ₀ -Q ₇	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ573SC 74LVQ573SCX	74LVQ573SJ 74LVQ573SJX	74LVQ573QSC 74LVQ573QSCX
See NS Package Number	M20B	M20D	MQA20

Functional Description

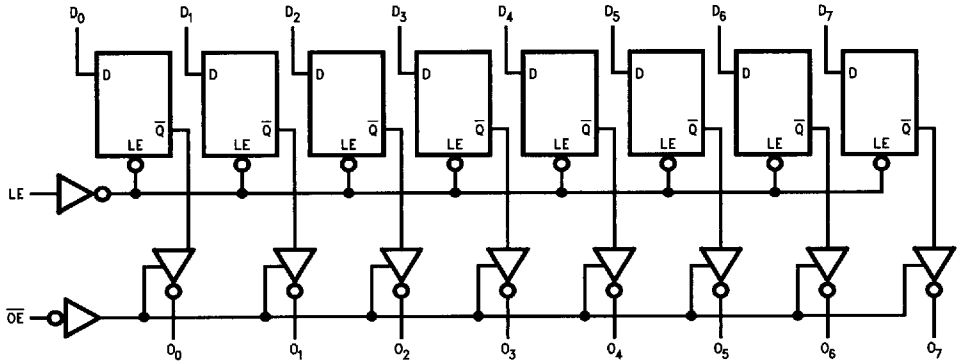
The LVQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are enabled. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
\overline{OE}	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
 L = LOW Voltage
 Z = High Impedance
 X = Immaterial
 O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



TL/F/11361-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	± 400 mA
Storage Temperature (T_{STG})	-65°C to +150°C
DC Latch-Up Source or Sink Current	± 300 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
LVQ	
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
V_{IN} from 0.8V to 2.0V	
$V_{CC} @ 3.0V$	125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ573		74LVQ573		Units	Conditions
			$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		3.0		2.58	2.48	V	* $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$	
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		3.0		0.36	0.44	V	* $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$	
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	± 1.0	μA	$V_I = V_{CC}, \text{GND}$	

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	74LVQ573		74LVQ573		Units	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	3.6			36		mA	V _{OLD} = 0.8 V _{Max} (Note 1)
I _{OHD}		3.6			-25		mA	V _{OHD} = 2.0V V _{Min} (Note 1)
I _{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0		μA	V _{IN} = V _{CC} or GND
I _{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5		μA	V _{I(OE)} = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.4	0.8			V	(Notes 2, 3)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.4	-0.8			V	(Notes 2, 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0			V	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	74LVQ573			74LVQ573		Units
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
t _{PHL}	Propagation Delay D _n to O _n	2.7	2.5	10.2	14.8	2.5	16.0	ns
t _{PLH}		3.3 ± 0.3	2.5	8.5	10.5	2.5	11.0	
t _{PLH}	Propagation Delay LE to O _n	2.7	2.5	10.2	16.9	2.5	18.0	ns
t _{PHL}		3.3 ± 0.3	2.5	8.5	12.0	2.5	12.5	
t _{PZL}	Output Enable Time	2.7	2.5	10.2	18.3	2.5	19.0	ns
t _{PZH}		3.3 ± 0.3	2.5	8.5	13.0	2.5	13.5	
t _{PHZ}	Output Disable Time	2.7	1.0	10.8	20.4	1.0	21.0	ns
t _{PLZ}		3.3 ± 0.3	1.0	9.0	14.5	1.0	15.0	
t _{OSSL}	Output to Output Skew*	2.7		1.0	1.5		1.5	ns
t _{OSLH}		3.3 ± 0.3		1.0	1.5		1.5	

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSSL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	74LVQ573		74LVQ573		Units
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _S	Setup Time, HIGH or LOW D _n to LE	2.7 3.3 ± 0.3	0	4.0	4.5	ns	
			0	3.0	3.0		
t _H	Hold Time, HIGH or LOW D _n to LE	2.7 3.3 ± 0.3	0	1.5	1.5	ns	
			0	1.5	1.5		
t _W	LE Pulse Width, HIGH	2.7 3.3 ± 0.3	2.4	5.0	6.0	ns	
			2.0	4.0	4.0		

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	37	pF	V _{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.