National Semiconductor

74LVQ273
Low Voltage Octal D Flip-Flop

General Description

The LVQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

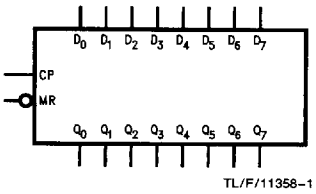
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Logic Symbols



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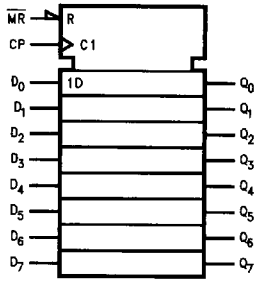
IEEE/IEC



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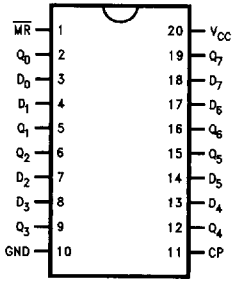
Connection Diagram

Pin Assignment for SOIC and QSOP



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Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ273SC 74LVQ273SCX	74LVQ273SJ 74LVQ273SJX	74LVQ273QSC 74LVQ273QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±400 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
LVQ	2.0V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74LVQ	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ273 T_A = +25°C		74LVQ273 T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		3.0		2.58	2.48	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −12 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 12 mA
I_{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	74LVQ273 $T_A = +25°C$ Typ	74LVQ273 $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	3.6		36	mA	V_{OLD} = 0.8V Max (Note 1)
I_{OHD}		3.6		−25	mA	V_{OHD} = 2.0V Min (Note 1)
I_{CC}	Maximum Quiescent Supply Current	3.6	4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8	V	(Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.3	−0.8	V	(Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ273 $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	74LVQ273 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
f_{max}	Maximum Clock Frequency	2.7 3.3 ±0.3	50 90			45 75		MHz
t_{PLH}	Propagation Delay CP to Q_n	2.7 3.3 ±0.3	4.0 4.0	9.6 8.0	17.6 12.5	3.0 3.0	20.0 14.0	ns
t_{PHL}	Propagation Delay CP to Q_n	2.7 3.3 ±0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.5 14.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	2.7 3.3 ±0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.0 14.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew*	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVQ273 $T_A = +25°C$, $C_L = 50$ pF		74LVQ273 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3		6.5 5.0	8.5 6.0	ns
t_h	Hold Time, HIGH or LOW D_n to CP	2.7 3.3 ±0.3		0.0 0.0	0.0 0.0	ns
t_w	Clock Pulse Width HIGH or LOW	2.7 3.3 ±0.3		7.0 5.5	8.5 6.0	ns
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	2.7 3.3 ±0.3		7.0 5.5	8.5 6.0	ns
t_w	Recovery Time $\overline{MR}$ to CP	2.7 3.3 ±0.3		5.0 4.0	6.5 4.5	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD} (Note 1)	Power Dissipation Capacitance	35	pF	V_{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.