

74LS621, LS622 Transceivers

'LS621 Non-Inverting Octal Bus Transceiver (Open Collector)
'LS622 Inverting Octal Bus Transceiver (Open Collector)
Product Specification

Logic Products

FEATURES

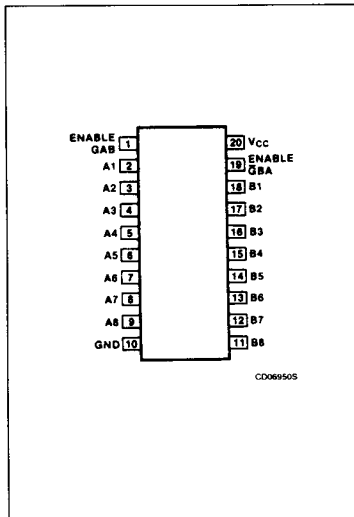
- Octal bidirectional bus interface
- Open-collector output
 - LS621, non-inverting
 - LS622, inverting
- Hysteresis on all Data inputs
- PNP inputs for reduced loading

DESCRIPTION

The 'LS621 is an octal transceiver featuring non-inverting open-collector bus compatible outputs in both send and receive directions. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'LS622 is an inverting version of the 'LS621. Both have built-in hysteresis to minimize ac noise effects.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

PIN CONFIGURATION



ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS621N, N74LS622N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
All	Outputs	30LSul

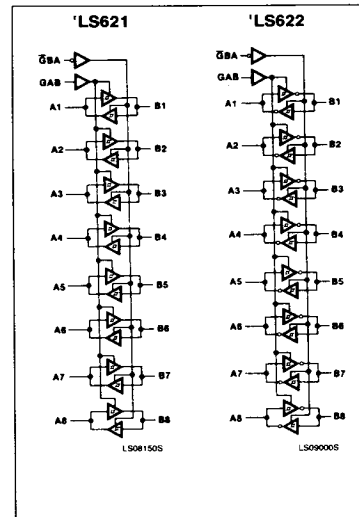
NOTE:

A 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{OL}$.

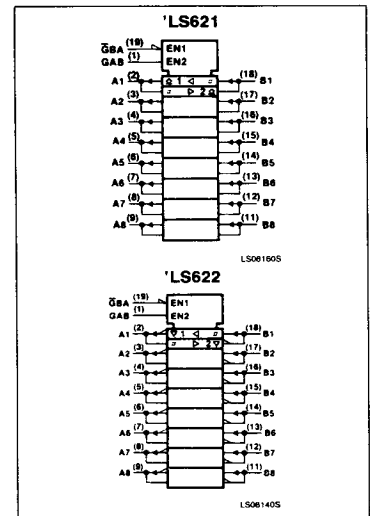
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the

logic levels at the enable inputs (\overline{GBA} and GAB).

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
		'LS621	'LS622
$\bar{G}BA$	GAB		
L	L	B data to A bus	\bar{B} data to A bus
H	H	A data to B bus	\bar{A} data to B bus
H	L	(Z)	(Z)
L	H	B data to A bus, A data to B bus	\bar{B} data to A bus, \bar{A} data to B bus

H = HIGH voltage level

L = LOW voltage level

(Z) = HIGH impedance (off) state

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS621 and 'LS622 the capability to store data by simultaneous enabling of $\bar{G}BA$ and GAB . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.6	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	HIGH-level output voltage			5.5	V
I_{OL}	LOW-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS621, 74LS622			UNIT
		Min	Typ ²	Max	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input	0.2	0.4		V
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{OH} = 5.5V$			100	μA
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12mA$	0.25	0.4	V
		$I_{OL} = 24mA$ (74LS)	0.35	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-1.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0V$			0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7V$			20	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4V$			-0.4	mA
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	42	70	mA
		I_{CCL} Outputs LOW	67	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

3. Measure I_{CC} with outputs open.

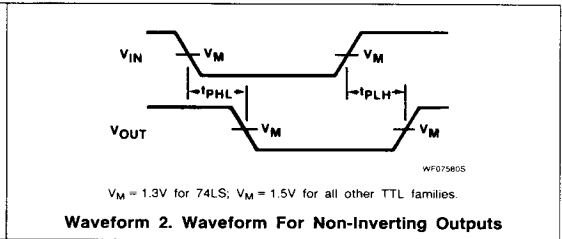
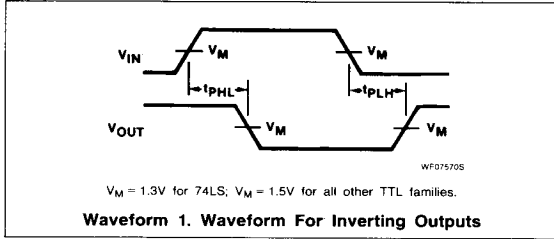
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	74LS621		74LS622		UNIT
		$C_L = 45pF$, $R_L = 667\Omega$		$C_L = 45pF$, $R_L = 667\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A input to B output	Waveform 2, '621 Waveform 1, '622		25 25		25 25	ns
t_{PLH} Propagation delay t_{PHL} B input to A output	Waveform 2, '621 Waveform 1, '622		25 25		25 25	ns
t_{PLH} Propagation delay $\bar{G}BA$ input to A output GAB input to B output	Waveform 1 Waveform 2		40 40		40 40	ns
t_{PHL} Propagation delay $\bar{G}BA$ input to A output GAB input to B output	Waveform 2 Waveform 1		50 50		60 60	ns

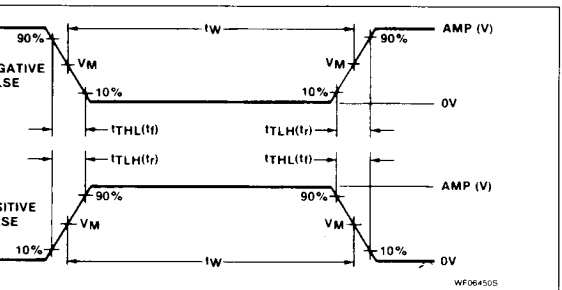
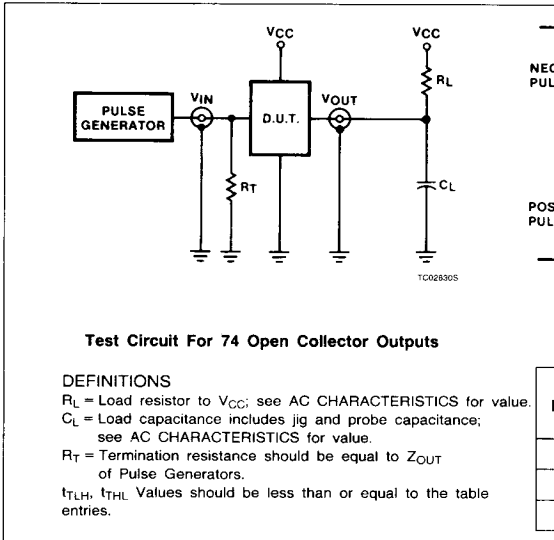
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AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns