T54LS568/569
T74LS568/569

PRELIMINARY DATA

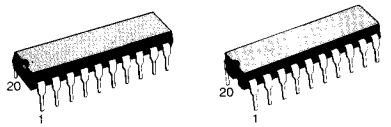
FOUR-BIT UP/DOWN COUNTERS WITH 3-STATE OUTPUTS

DESCRIPTION

The T54LS/T74LS568/569 is designed as programmable up/down BCD; the T54LS/T74LS569 as a Binary counter. Both have 3-state outputs to be used in bus organised system. All functions (except for output enable ($\overline{OE}$) and synchronous clear ($\overline{ACLR}$) occur on the positive edge of the clock pulse (CP).

When the $\overline{LOAD}$ input is LOW, the outputs are programmed by the parallel data inputs (A, B, C, D) on the next clock edge. The counters are enabled only when $\overline{CEP}$ and $\overline{CET}$ are LOW and LOAD is HIGH.

Direction of the count is controlled by the up/down input (U/$\overline{D}$), while HIGH counts up an LOW counts down. High - speed counting and cascading are put into effect by internal look-ahead carry logic and an active LOW ripple carry output ($\overline{RCO}$). On the LS568 during up-count the $\overline{RCO}$ is LOW at binary 9 and during down-count it is LOW at binary 0. On the LS569 during up-count the $\overline{RCO}$ is LOW at binary 15 and during down-count it is LOW at binary O.During normal cascading operation $\overline{RCO}$ connected to the succeeding block at $\overline{CET}$ is the only requisite. When counting and when $\overline{RCO}$ is LOW, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse. Two active LOW reset lines are provided, a master reset equal to the LOW time of the clock pulse. Two active LOW reset lines are provided, a master reset asynchronous clear ($\overline{ACLR}$) and synchronous clear ($\overline{SCLR}$). When in a HIGH state, the output control ($\overline{OE}$) input forces the counter output into a HIGH impendance state and when LOW, the counter outputs are enabled.



B1
Plastic Package

D1/D2
Ceramic Package

M1
Micro Package

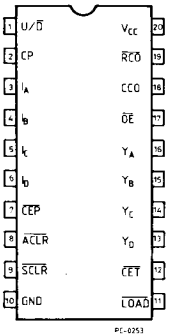
C1
Plastic Chip Carrier

ORDERING NUMBERS:

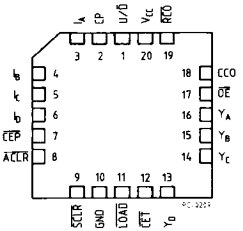
T54LSXXX D2	T74LSXXX C1
T74LSXXX D1	T74LSXXX M1
T74LSXXX B1	

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

FUNCTION TABLE

INPUTS												OUTPUTS						
CP	D	C	B	A	$\overline{LOAD}$	$\overline{CET}$	$\overline{CEP}$	V/$\overline{D}$	$\overline{ACLR}$	$\overline{SCLR}$	$\overline{OE}$	$\overline{RCO}$	CCO	Y_D	Y_C	Y_B	Y_A	
↑	X	X	X	X	H	L	L	H	H	H	L	A/R	A/R	(Q_T—CP)-1				Count Up
↑	X	X	X	X	H	L	L	L	H	H	L	A/R	A/R	(Q_T—CP)-1				Count Down
↑	X	X	X	X	H	H	X	X	H	H	L	H	H	NC	NC	NC	NC	Count Inhibit
↑	X	X	X	X	H	L	H	X	H	H	L	A/R	H	NC	NC	NC	NC	Count Inhibit
⊓	X	X	X	X	X	L	L	H	H	H	L	L	⊓	H	H	H	H	Overflow (LS569)
↑	X	X	X	X	X	L	H	H	H	H	L	L	H	H	H	H	H	Overflow (LS569)
⊓	X	X	X	X	X	L	L	H	H	H	L	L	⊓	H	L	L	H	Overflow (LS658)
↑	X	X	X	X	X	L	H	H	H	H	L	L	H	H	L	L	H	Overflow (LS568)
↑	X	X	X	X	X	H	X	H	H	H	L	H	H	H	H	H	H	Overflow Inhibit (LS569)
↑	X	X	X	X	X	H	X	H	H	H	L	H	H	H	L	L	H	Overflow Inhibit (LS568)
⊓	X	X	X	X	X	L	L	L	H	H	L	L	⊓	L	L	L	L	Underflow
↑	X	X	X	X	X	L	H	L	H	H	L	L	H	L	L	L	L	Underflow
↑	X	X	X	X	X	H	X	L	H	H	L	H	H	L	L	L	L	Underflow inhibit
↑	L	H	L	H	L	X	X	X	H	H	L	H	H	L	H	L	H	Load Esample
↑	X	X	X	X	X	X	X	H	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
⊓	X	X	X	X	X	L	L	L	H	L	L	L	⊓	L	L	L	L	Clear (Synchronous)
↑	X	X	X	X	X	L	H	L	H	L	L	L	H	L	L	L	L	Clear (Synchronous)
↑	X	X	X	X	X	H	X	L	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
X	X	X	X	X	X	X	X	H	L	X	L	H	H	L	L	L	L	Asynchronous Clear
⊓	X	X	X	X	X	L	L	L	L	X	L	L	⊓	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	L	H	L	L	X	L	L	H	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	H	X	L	L	X	L	H	H	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	X	X	X	X	X	H	X	X	Hi-Z				Output Disabled

(Q_T—CP) = Output state prior to clock edge
NC = No change
A/R = Assumes required output state: High except during Overflow and Underflow
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

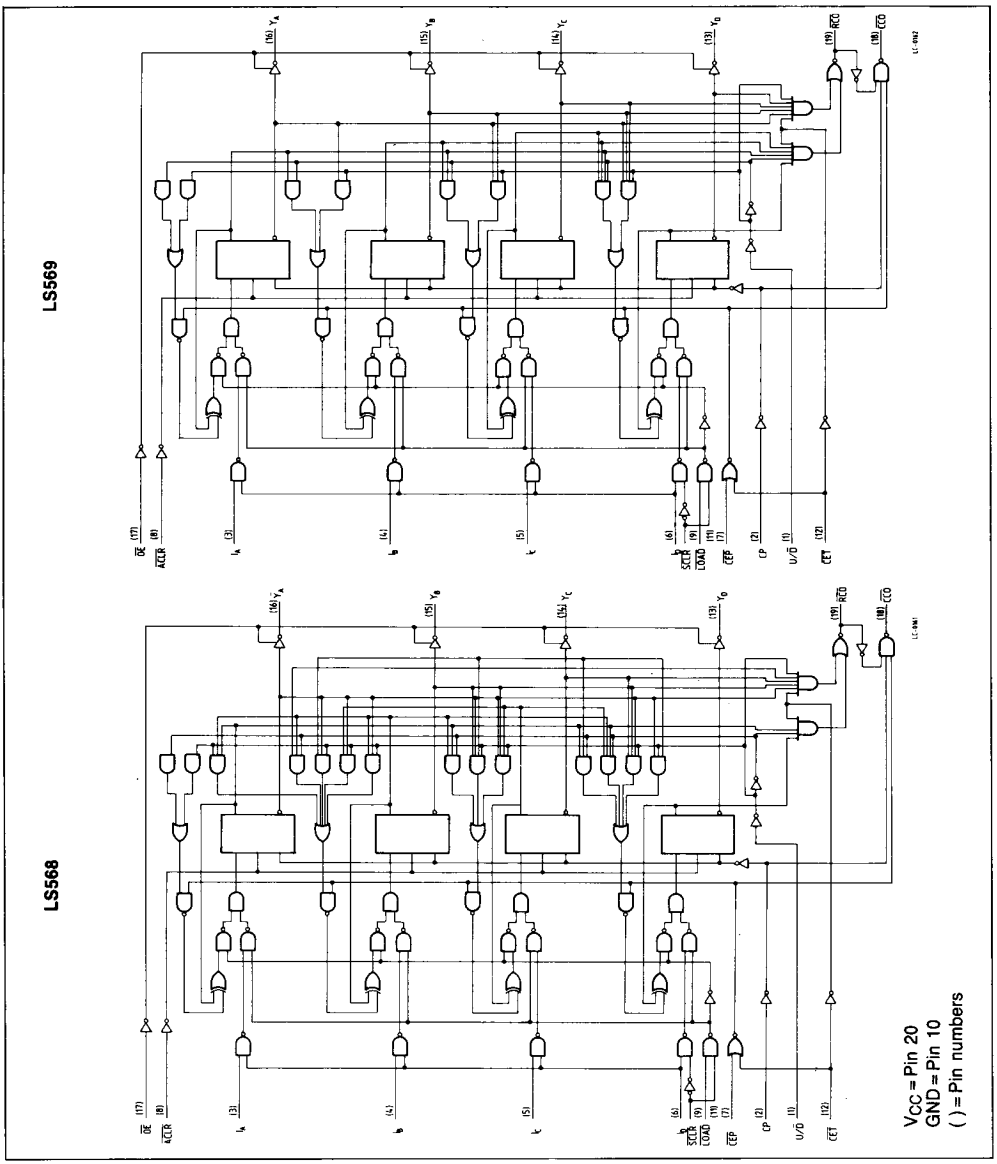
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS568/569D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS568/569XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

LOGIC DIAGRAMS



DEFINITION OF FUNCTIONAL TERMS

A, B, C, D The four programmable data inputs.

$\overline{CEP}$ Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. $\overline{CEP}$ must be LOW to count.

$\overline{CET}$ Count Enable Trickie. Enables the ripple carry output for cascaded operation. Must be LOW to count.

CP Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.

$\overline{LOAD}$ Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.

U/$\overline{D}$ Up/Down Count Contro HIGH counts up and LOW counts down.

$\overline{ACLR}$ Asynchronous Clear, Master reset of counters to zero when $\overline{ACLR}$ is LOW, independent of the clock.

$\overline{SCLR}$ Synchronous clear of counters to zero on the next clock edge when $\overline{SCLR}$ is LOW.

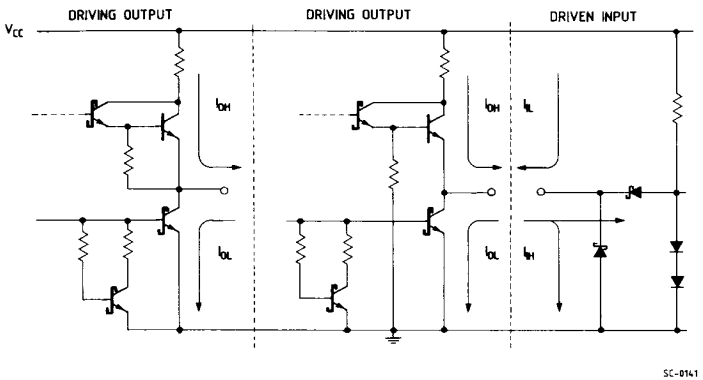
$\overline{OE}$ A HIGH on the output contro sets the four counter outputs in the high impedance, and a LOW, enables the output.

Y_A, Y_B, Y_C, Y_D The Four counter outputs.

$\overline{RCO}$ Ripple Carry Output. Output will be LOW on the maximum count on up-count. Up down-count. $\overline{RCO}$ is LOW at 0000.

CCO Clock Carry Output. Wile counting and $\overline{RCO}$ is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

Low-Power Schottky Input/Output
Current Interface Conditions



Note: Actual current flow direction shown.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage $\overline{RCO}$, CCO	54	2.4	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.4	3.1			
		54	2.5	3.5			
		74	2.7	3.5			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA; V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table	V
		74		0.35	0.5	I_{OL} = 24mA	
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_O = 2.7V	μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_O = 2.4V	μA
I_{IH}	Input HIGH Current				20	V_{CC} = MAX, V_{IN} = 2.7V	μA
					0.1	V_{CC} = MAX, V_{IN} = 7.0V	mA
I_{IL}	Input LOW Current	Others			−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
		$\overline{CET}$			−0.8		
I_{OS}	Output Short Circuit Current (Note 2)						
	$\overline{RCO}$, CCO		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
	Others		−30		−130		
I_{CC}	Power Supply Current 3-State				43	V_{CC} = MAX	mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions	Units
t_W	Clock Pulse Width	30			V_{CC} = 5.0V	ns
t_s	Set-up Time, A, B, C, D	20				ns
t_s	Set-up Time, $\overline{SCRL}$	20				ns
t_s	Set-up Time, $\overline{LOAD}$	30				ns
t_s	Set-up Time, U/$\overline{D}$	50				ns
t_s	Set-up Time, $\overline{CET}$, $\overline{CEP}$	32				ns
t_h	Hold Time, Any Inputs	0				ns

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Maximum Toggle Frequency	25			$V_{CC} = 5.0V$ $C_L = 15pF$	MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Q		15 23	24 35		ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{RCO}$		14 14	24 24		ns
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{RCO}$		20 15	30 24		ns
t_{PLH} t_{PHL}	Propagation Delay Clock to $\overline{RCO}$		25 26	40 40		ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ or $\overline{CEP}$ to CCO		12 20	20 30		ns
t_{PLH} t_{PHL}	Propagation Delay Clock to CCO		17 26	27 40		ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{ACLR}$ to Q		21 21	32 32		ns
t_{PZH} t_{PZL}	Output Enable Time		10 17	16 24		ns
t_{PHZ} t_{PLZ}	Output Disable Time		20 17	25 27	$C_L = 5.0pF$	ns

MICROPROGRAMMABLE DUAL-EVENT 8-BIT COUNTERS