

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT564

Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

Product specification
File under Integrated Circuits, IC06

December 1990

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74HC/HCT564

FEATURES

- 3-state inverting outputs for bus oriented applications
- 8-bit positive-edge triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT564 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT564 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable (\overline{OE}) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When \overline{OE} is LOW, the contents of the 8 flip-flops are available at the outputs.

When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

The "564" is functionally identical to the "574" but has inverting outputs. The "564" is functionally identical to the "534", but has a different pinning.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|------------------------------------|---|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} /t _{PLH} | propagation delay CP to \overline{Q}_n | C _L = 15 pF; V _{CC} = 5 V | 15 | 16 | ns |
| f _{max} | maximum clock frequency | | 127 | 62 | MHz |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per flip-flop | notes 1 and 2 | 27 | 27 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}; for HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING INFORMATION

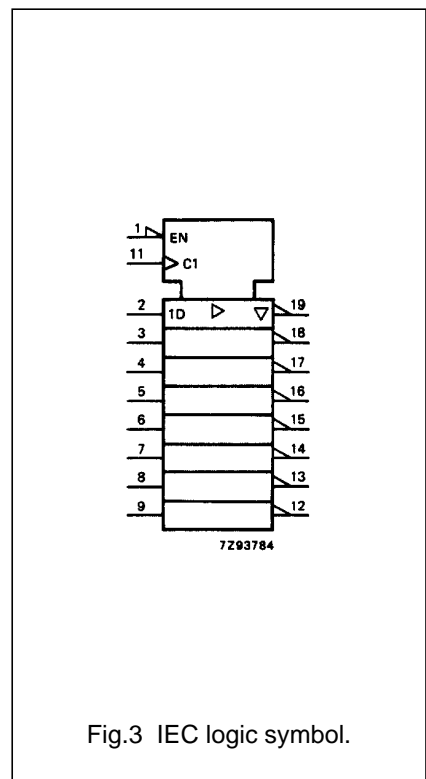
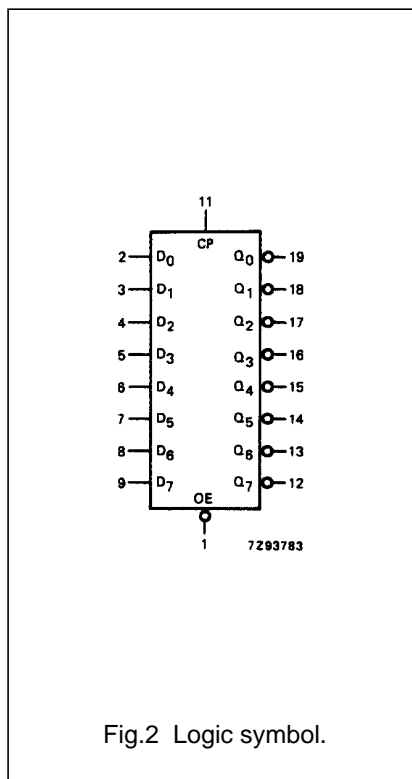
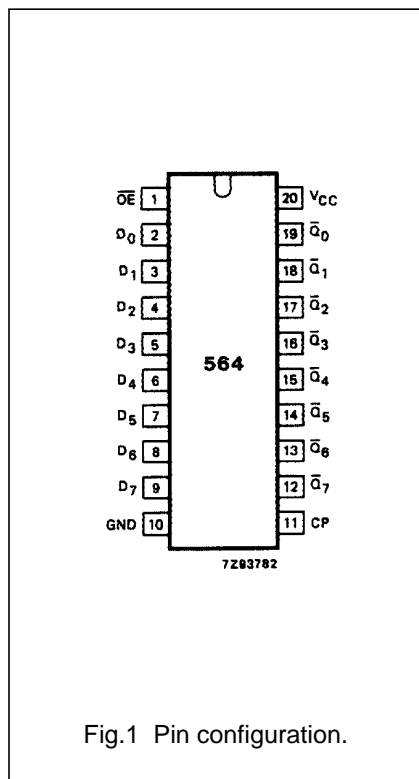
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Octal D-type flip-flop; positive-edge trigger;
3-state; inverting

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------------------------|--------------------------------------|---|
| 1 | \overline{OE} | 3-state output enable input (active LOW) |
| 2, 3, 4, 5, 6, 7, 8, 9 | D ₀ to D ₇ | data inputs |
| 10 | GND | ground (0 V) |
| 11 | CP | clock input (LOW-to-HIGH, edge-triggered) |
| 19, 18, 17, 16, 15, 14, 13, 12 | \overline{Q}_0 to \overline{Q}_7 | 3-state flip-flop outputs |
| 20 | V _{CC} | positive supply voltage |



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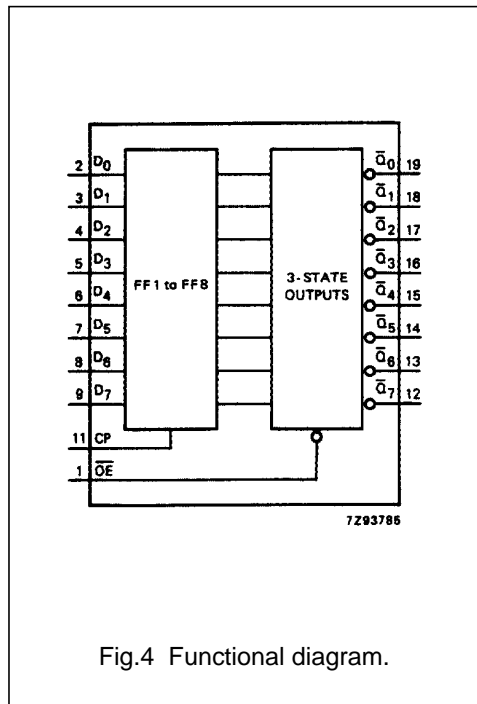


Fig.4 Functional diagram.

FUNCTION TABLE

| OPERATING MODES | INPUTS | | | INTERNAL FLIP-FLOPS | OUTPUTS |
|-----------------------------------|-----------------|------------|-------|---------------------|--------------------------------------|
| | \overline{OE} | CP | D_n | | \overline{Q}_0 to \overline{Q}_7 |
| load and read register | L | \uparrow | l | L | H |
| register | L | \uparrow | h | H | L |
| load register and disable outputs | H | \uparrow | l | L | Z |
| | H | \uparrow | h | H | Z |

Notes

- H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
 \uparrow = LOW-to-HIGH clock transition

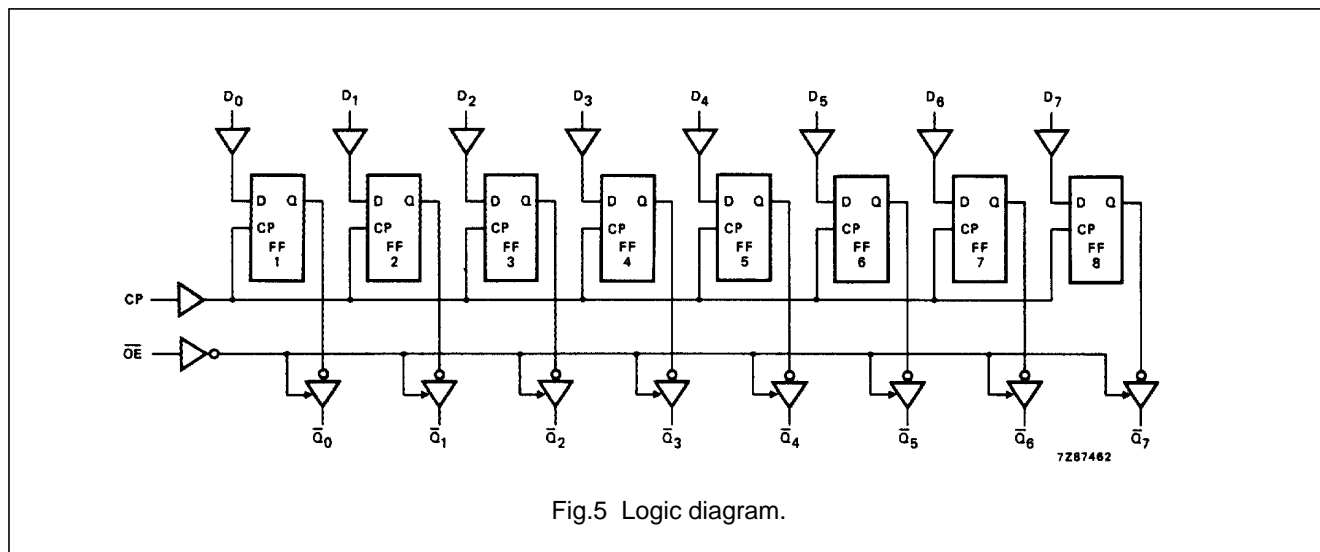


Fig.5 Logic diagram.

Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay CP to \bar{Q}_n | | 50 18 14 | 165 33 28 | | 205 41 35 | | 250 50 43 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PZH} / t _{PZL} | 3-state output enable time \bar{OE} to \bar{Q}_n | | 44 16 13 | 140 28 24 | | 175 35 30 | | 210 42 36 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time \bar{OE} to \bar{Q}_n | | 50 18 14 | 135 27 23 | | 170 34 29 | | 205 41 35 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{THL} / t _{TLH} | output transition time | | 14 5 4 | 60 12 10 | | 75 15 13 | | 90 18 15 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _W | clock pulse width HIGH or LOW | 80 16 14 | 14 5 4 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{SU} | set-up time D _n to CP | 60 12 10 | 6 2 2 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig.7 |
| t _H | hold time D _n to CP | 5 5 5 | 0 0 0 | | 5 5 5 | | 5 5 5 | | ns | 2.0 4.5 6.0 | Fig.7 |
| f _{max} | maximum clock pulse frequency | 6.0 30 35 | 38 115 137 | | 4.8 24 28 | | 4.0 20 24 | | MHz | 2.0 4.5 6.0 | Fig.6 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|----------------------------------|-----------------------|
| \overline{OE} | 0.80 |
| D ₀ to D ₇ | 0.25 |
| CP | 1.00 |

AC CHARACTERISTICS FOR 74HCT

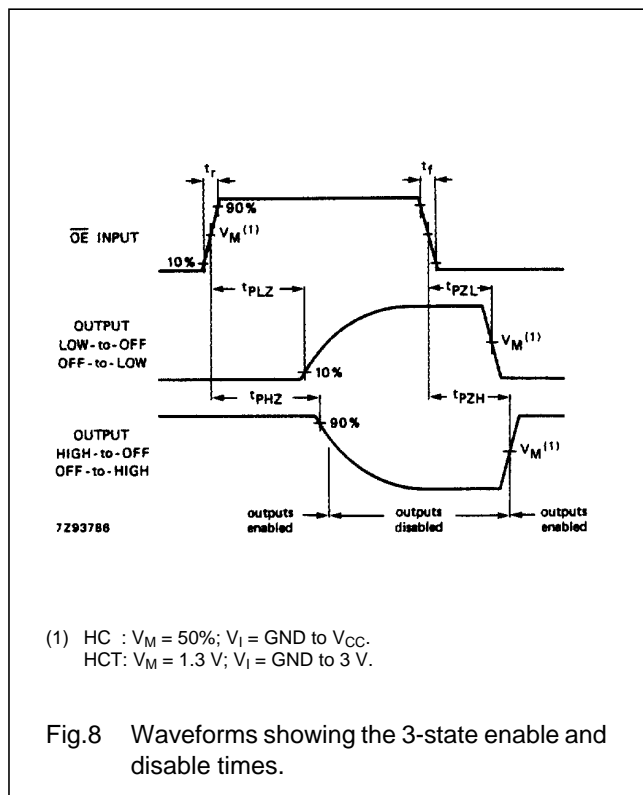
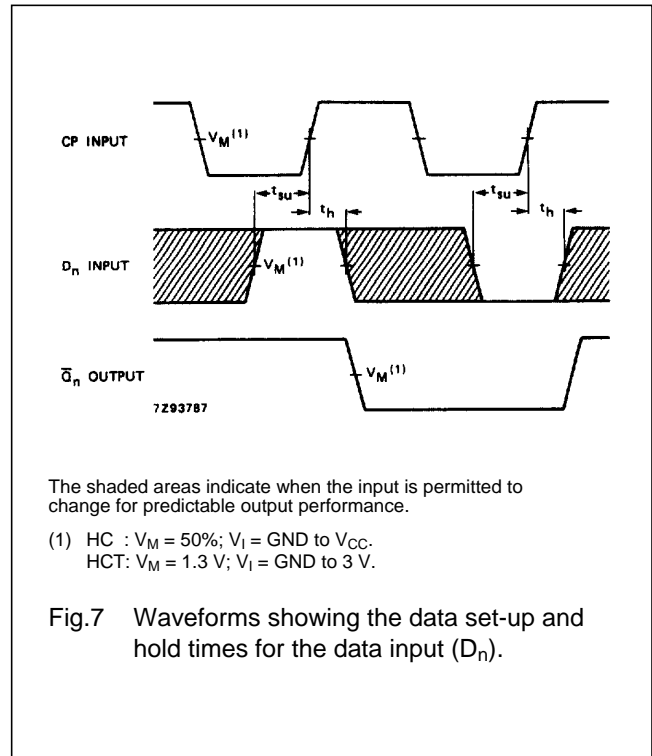
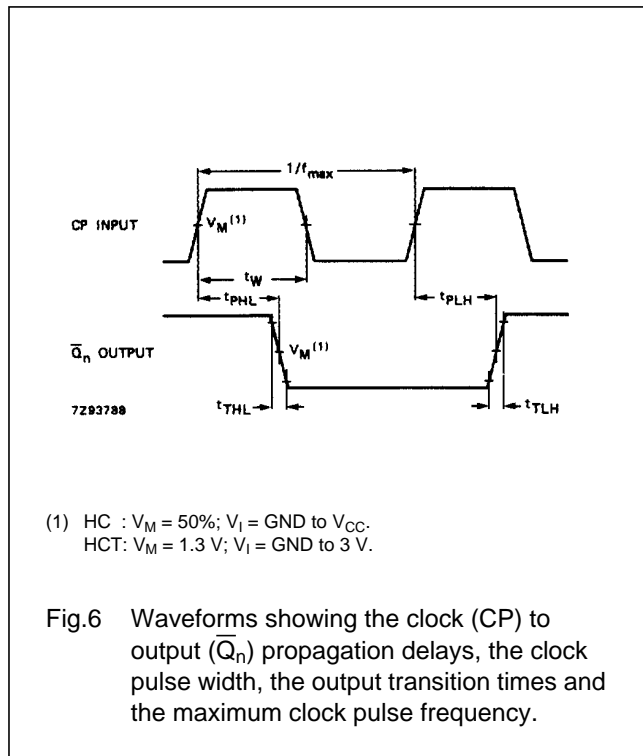
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|------------------------|-----------|-------|
| | | 74HCT | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay CP to \overline{Q}_n | | 19 | 35 | | 44 | | 53 | ns | 4.5 | Fig.6 |
| t _{PZH} / t _{PZL} | 3-state output enable time OE to \overline{Q}_n | | 19 | 35 | | 44 | | 53 | ns | 4.5 | Fig.8 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time \overline{OE} to \overline{Q}_n | | 19 | 30 | | 38 | | 45 | ns | 4.5 | Fig.8 |
| t _{THL} / t _{TLH} | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig.6 |
| t _W | clock pulse width HIGH or LOW | 18 | 8 | | 23 | | 27 | | ns | 4.5 | Fig.6 |
| t _{SU} | set-up time D _n to CP | 12 | 3 | | 15 | | 18 | | ns | 4.5 | Fig.7 |
| t _H | hold time D _n to CP | 3 | -2 | | 3 | | 3 | | ns | 4.5 | Fig.7 |
| f _{max} | maximum clock pulse frequency | 27 | 56 | | 22 | | 18 | | MHz | 4.5 | Fig.6 |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".