

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT253**

**Dual 4-input multiplexer; 3-state**

Product specification  
File under Integrated Circuits, IC06

December 1990

## Dual 4-input multiplexer; 3-state

## 74HC/HCT253

## FEATURES

- Non-inverting data path
- 3-state outputs for bus interface
- and multiplex expansion
- Common select inputs
- Separate output enable inputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT253 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT253 have two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common data select inputs ( $S_0, S_1$ ).

When the individual output enable ( $1\overline{OE}, 2\overline{OE}$ ) inputs of the 4-input multiplexers are HIGH, the outputs are forced to the high impedance OFF-state. The "253" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to  $S_0$  and  $S_1$ .

The logic equations for the outputs are:

$$1Y = 1\overline{OE}(1I_0.\overline{S_1}.\overline{S_0}+1I_1.\overline{S_1}.S_0+1I_2.S_1.\overline{S_0}+1I_3.S_1.S_0)$$

$$2Y = 2\overline{OE}(2I_0.\overline{S_1}.\overline{S_0}+2I_1.\overline{S_1}.S_0+2I_2.S_1.\overline{S_0}+2I_3.S_1.S_0)$$

## APPLICATIONS

- Data selectors
- Data multiplexers

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> , 2I <sub>n</sub> to nY; S <sub>n</sub> to nY	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	17 18	17 19	ns ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per multiplexer	notes 1 and 2	55	55	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>i</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>i</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

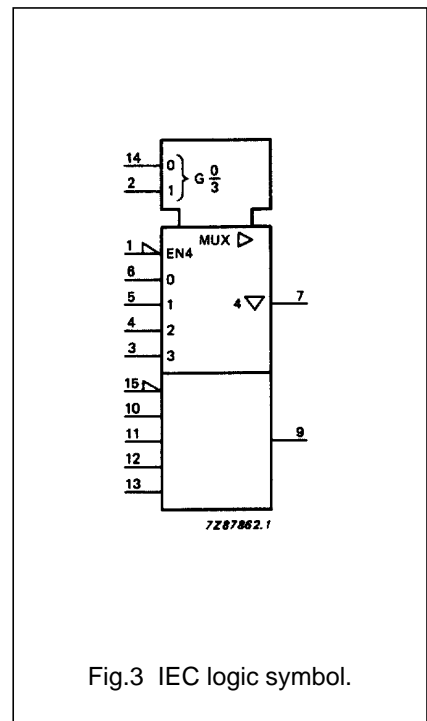
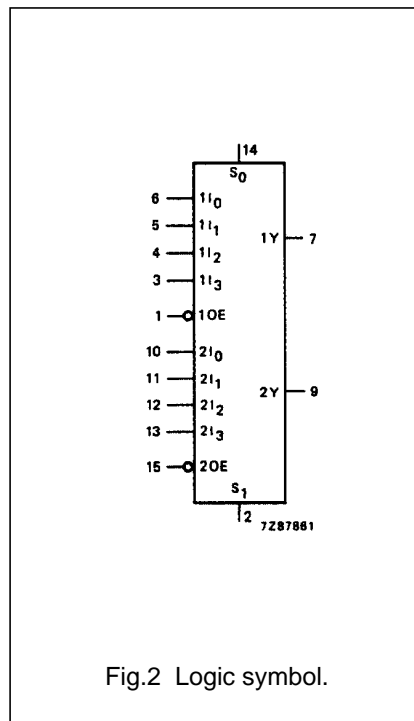
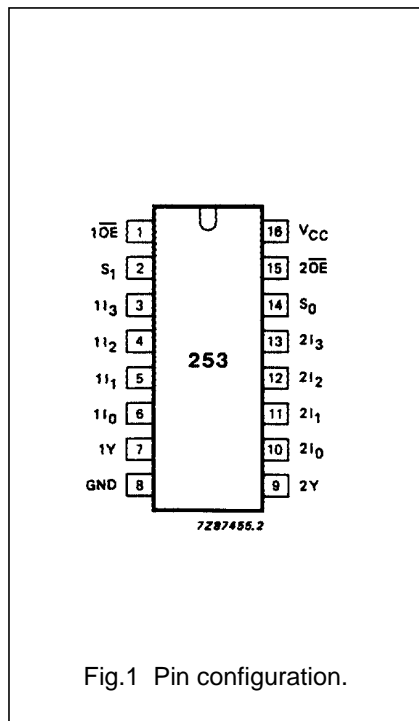
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{1OE}, \overline{2OE}$	output enable inputs (active LOW)
14, 2	$S_0, S_1$	common data select inputs
7, 9	1Y, 2Y	3-state multiplexer outputs
8	GND	ground (0 V)
6, 5, 4, 3	1I <sub>0</sub> to 1I <sub>3</sub>	data inputs from source 1
10, 11, 12, 13	2I <sub>0</sub> to 2I <sub>3</sub>	data inputs from source 2
16	V <sub>CC</sub>	positive supply voltage



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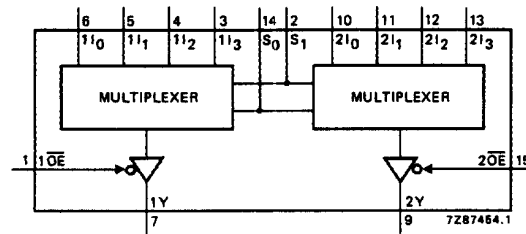


Fig.4 Functional diagram.

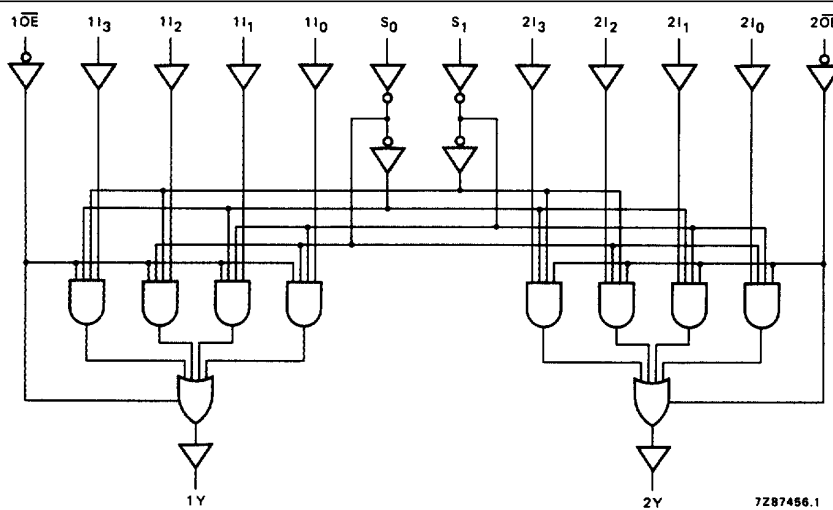


Fig.5 Logic diagram.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S <sub>0</sub>	S <sub>1</sub>	nI <sub>0</sub>	nI <sub>1</sub>	nI <sub>2</sub>	nI <sub>3</sub>	nOE	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

NOTES

- H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

## Dual 4-input multiplexer; 3-state

## 74HC/HCT253

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to nY		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time n $\overline{\text{OE}}$ to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time n $\overline{\text{OE}}$ to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1I <sub>n</sub>	0.40
2I <sub>n</sub>	0.40
n $\overline{OE}$	1.10
S <sub>0</sub>	1.10
S <sub>1</sub>	1.10

**AC CHARACTERISTICS FOR 74HCT**

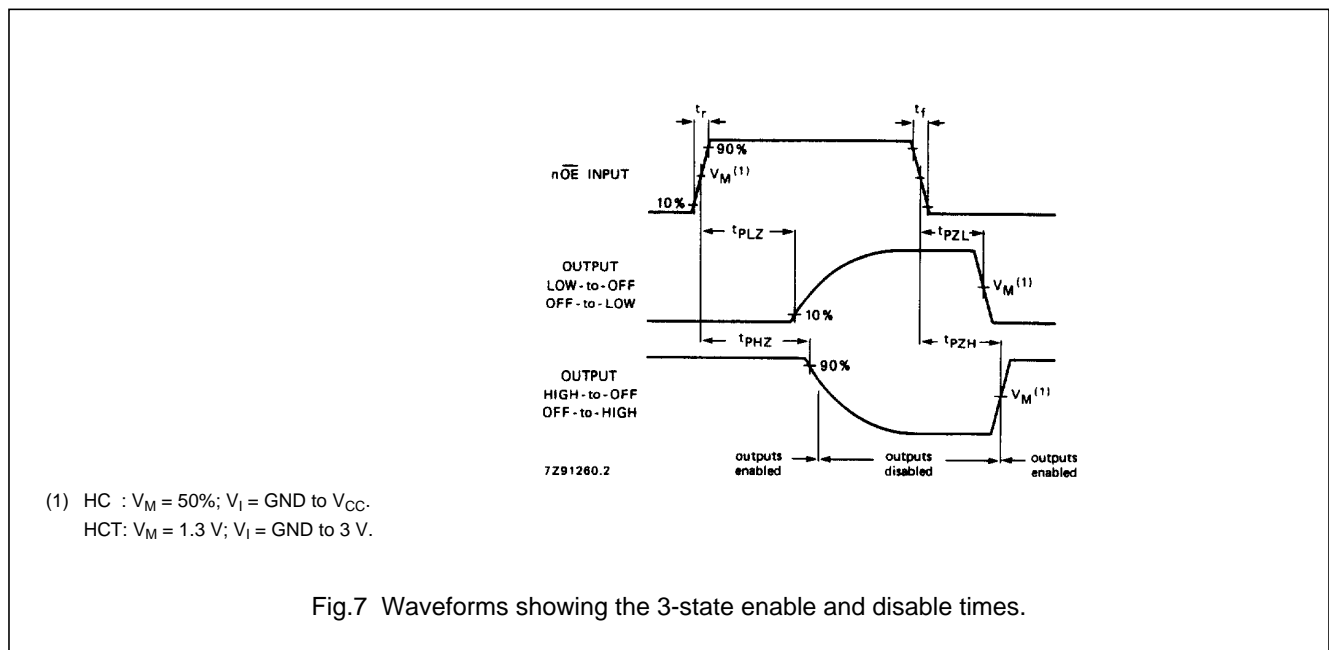
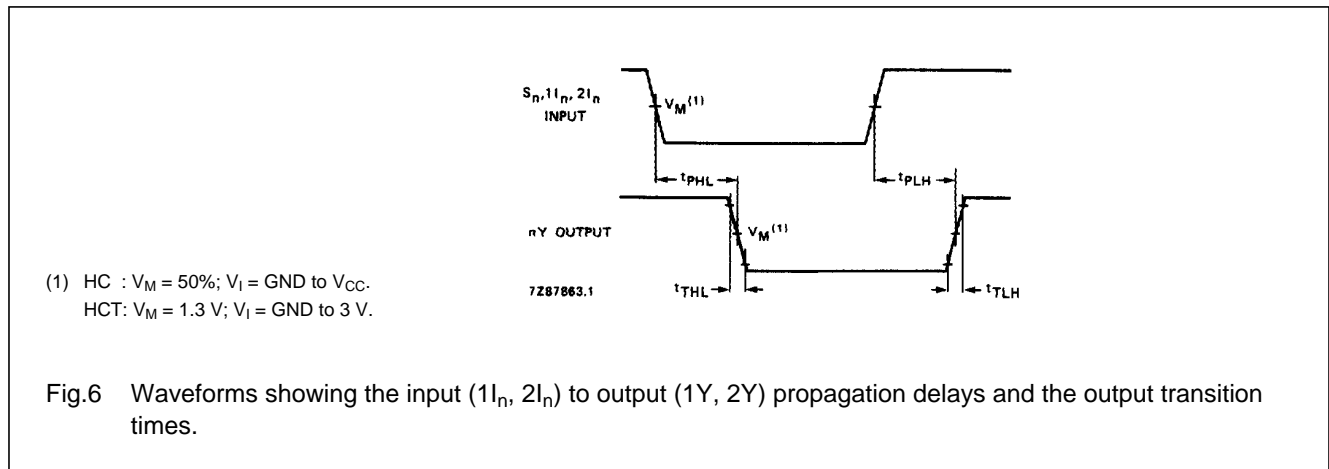
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1I <sub>n</sub> to nY; 2I <sub>n</sub> to nY		20	38		48		57	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>n</sub> to nY		22	40		50		60	ns	4.5	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time n $\overline{OE}$ to nY		14	30		38		45	ns	4.5	Fig.7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time n $\overline{OE}$ to nY		13	30		38		45	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".