

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT10** Triple 3-input NAND gate

Product specification  
File under Integrated Circuits, IC06

December 1990

## Triple 3-input NAND gate

## 74HC/HCT10

## FEATURES

- Output capability: standard
- $I_{CC}$  category: SSI

## GENERAL DESCRIPTION

The 74HC/HCT10 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT10 provide the 3-input NAND function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER                              | CONDITIONS                                   | TYPICAL |     | UNIT |
|-------------------|--|--|---------|-----|------|
|                   |  |  | HC      | HCT |      |
| $t_{PHL}/t_{PLH}$ | propagation delay nA, nB, nC to nY     | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 9       | 11  | ns   |
| $C_I$             | input capacitance                      |  | 3.5     | 3.5 | pF   |
| $C_{PD}$          | power dissipation capacitance per gate | notes 1 and 2                                | 12      | 14  | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ .

## ORDERING INFORMATION

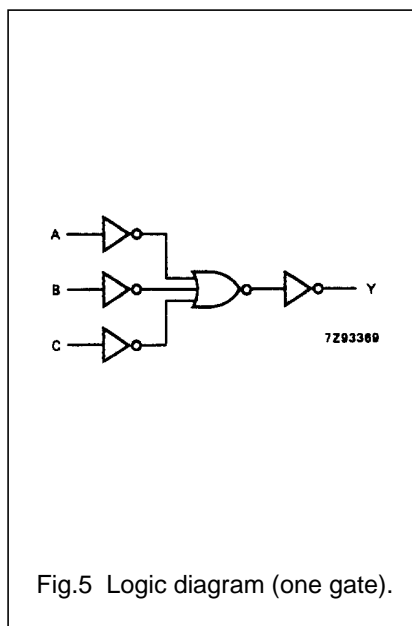
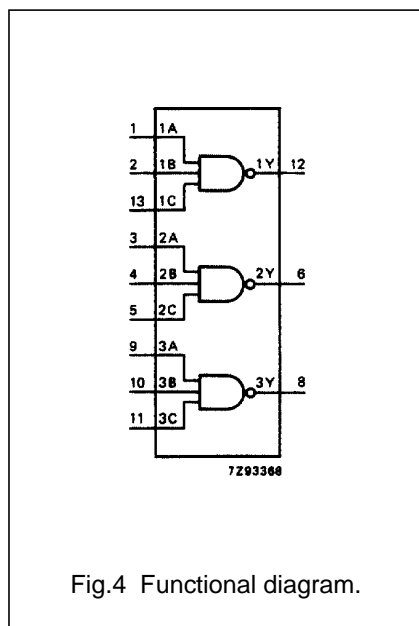
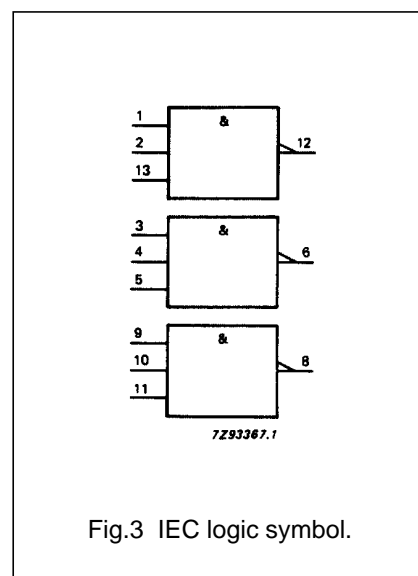
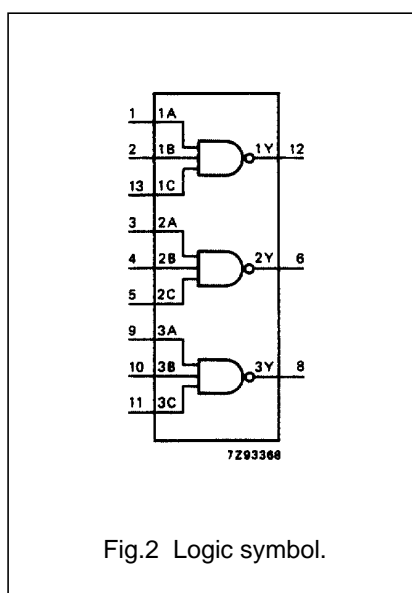
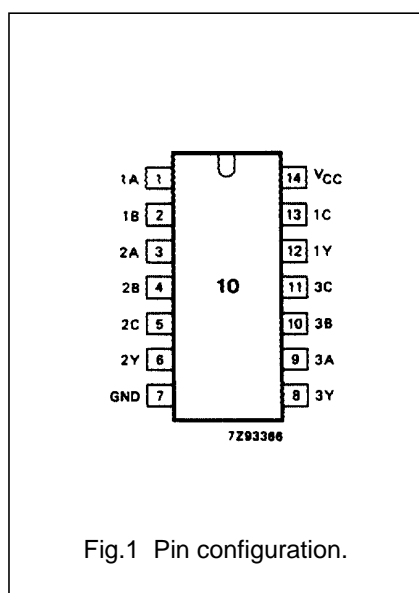
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# Triple 3-input NAND gate

# 74HC/HCT10

## PIN DESCRIPTION

| PIN NO.   | SYMBOL          | NAME AND FUNCTION       |
|-----------|-----------------|-------------------------|
| 1, 3, 9   | 1A to 3A        | data inputs             |
| 2, 4, 10  | 1B to 3B        | data inputs             |
| 13, 5, 11 | 1C to 3C        | data inputs             |
| 12, 6, 8  | 1Y to 3Y        | data outputs            |
| 7         | GND             | ground (0 V)            |
| 14        | V <sub>CC</sub> | positive supply voltage |



## FUNCTION TABLE

| INPUTS |    |    | OUTPUT |
|--------|----|----|--------|
| nA     | nB | nC | nY     |
| L      | L  | L  | H      |
| L      | L  | H  | H      |
| L      | H  | L  | H      |
| L      | H  | H  | H      |
| H      | L  | L  | H      |
| H      | L  | H  | H      |
| H      | H  | L  | H      |
| H      | H  | H  | L      |

### Notes

- H = HIGH voltage level  
L = LOW voltage level

## Triple 3-input NAND gate

## 74HC/HCT10

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: SSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                             | T <sub>amb</sub> (°C) |               |                |             |                 |              |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|---------------------------------------|-----------------------|---------------|----------------|-------------|-----------------|--------------|-----------------|------|------------------------|-----------|
|                                     |                                       | 74HC                  |               |                |             |                 |              |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                       | +25                   |               |                | -40 to + 85 |                 | -40 to + 125 |                 |      |                        |           |
|                                     |                                       | min.                  | typ.          | max.           | min.        | max.            | min.         | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA, nB, nC to nY |                       | 30<br>11<br>9 | 95<br>19<br>16 |             | 120<br>24<br>20 |              | 145<br>29<br>25 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                |                       | 19<br>7<br>6  | 75<br>15<br>13 |             | 95<br>19<br>16  |              | 110<br>22<br>19 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |

# Triple 3-input NAND gate

# 74HC/HCT10

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: SSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

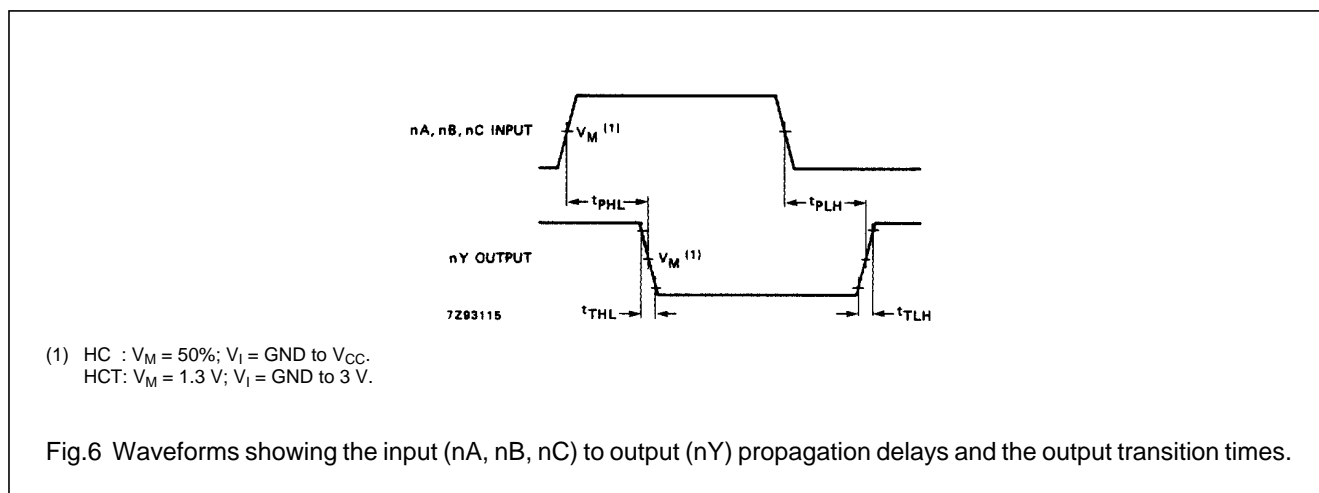
| INPUT      | UNIT LOAD COEFFICIENT |
|------------|-----------------------|
| nA, nB, nC | 1.5                   |

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                             | T <sub>amb</sub> (°C) |      |      |             |      |             | UNIT | TEST CONDITIONS     |           |       |
|-------------------------------------|---------------------------------------|-----------------------|------|------|-------------|------|-------------|------|---------------------|-----------|-------|
|                                     |                                       | 74HCT                 |      |      |             |      |             |      | V <sub>CC</sub> (V) | WAVEFORMS |       |
|                                     |                                       | + 25                  |      |      | -40 to + 85 |      | -40 to +125 |      |                     |           |       |
|                                     |                                       | min.                  | typ. | max. | min.        | max. | min.        |      |                     |           | max.  |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA, nB, nC to nY |                       | 14   | 24   |             | 30   |             | 36   | ns                  | 4.5       | Fig.6 |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                |                       | 7    | 15   |             | 19   |             | 22   | ns                  | 4.5       | Fig.6 |

## AC WAVEFORMS



## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.