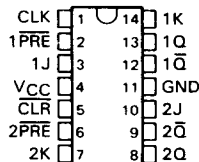


# SN54HC78, SN74HC78 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

D2084, DECEMBER 1982—REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC78 . . . J PACKAGE  
SN74HC78 . . . D OR N PACKAGE  
(TOP VIEW)



For functionally and electrically identical parts in chip carrier packages, see SN54HC114.

## description

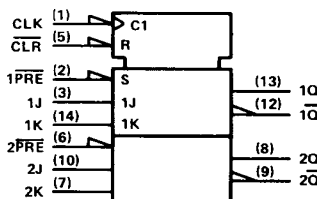
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When the Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>‡</sup>	H <sup>‡</sup>
H	H	I	L	L	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	I	H	L	H	L
H	H	I	L	H	L	H
H	H	I	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

<sup>‡</sup>This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

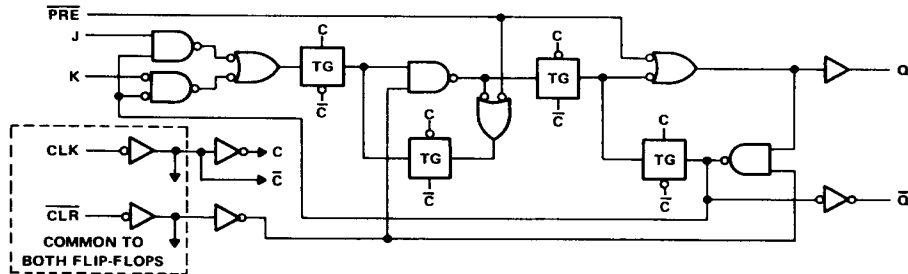
## logic symbol †



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

## logic diagram, each flip-flop (positive logic)



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# SN54HC78, SN74HC78 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

## absolute maximum ratings over operating free-air temperature range†

Supply voltage, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND pins	$\pm 50$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54HC78			SN74HC78			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage		2	5	6	2	5	6	V
$V_{IH}$ High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
	$V_{CC} = 4.5$ V	3.15			3.15			
	$V_{CC} = 6$ V	4.2			4.2			
$V_{IL}$ Low-level input voltage	$V_{CC} = 2$ V	0	0.3		0	0.3		V
	$V_{CC} = 4.5$ V	0	0.9		0	0.9		
	$V_{CC} = 6$ V	0	1.2		0	1.2		
$V_I$ Input voltage		0	$V_{CC}$		0	$V_{CC}$		V
$V_O$ Output voltage		0	$V_{CC}$		0	$V_{CC}$		V
$t_t$ Input transition (rise and fall) times	$V_{CC} = 2$ V	0	1000		0	1000		ns
	$V_{CC} = 4.5$ V	0	500		0	500		
	$V_{CC} = 6$ V	0	400		0	400		
$T_A$ Operating free-air temperature		-55	125		-40	85		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC78		SN74HC78		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30		3.7		3.84		
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.80		5.2		5.34		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
$I_I$	$V_I = V_{CC}$ or 0	6 V		$\pm 0.1$	$\pm 100$		$\pm 1000$		$\pm 1000$	nA
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V					4		80	$\mu\text{A}$
$C_i$		2 to 6 V		3	10		10		10	pF

**SN54HC78, SN74HC78**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH PRESET, COMMON CLEAR, AND COMMON CLOCK**

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC78		SN74HC78		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	0		6	0	4.2	0	5	MHz
		4.5 V	0		31	0	21	0	25	
		6 V	0		36	0	25	0	29	
t <sub>w</sub>	Pulse duration	CLR or PRE low	2 V	80		119		101		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLK high or low	2 V	80		119		101		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
t <sub>su</sub>	Setup time before CLK↓	CLR or PRE inactive or data	2 V	100		150		125		ns
			4.5 V	25		35		30		
			6 V	20		30		25		
t <sub>h</sub>	Hold time, data after CLK↓	2 V	0		0		0		ns	
		4.5 V	0		0		0			
		6 V	0		0		0			

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C<sub>L</sub> = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC78		SN74HC78		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	9		4.2		5	MHz	
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t <sub>pd</sub>	PRE or CLR	Q or Q̄	2 V		78	155		250		194	ns
			4.5 V		16	31		47		39	
			6 V		13	26		40		32	
t <sub>pd</sub>	CLK	Q or Q̄	2 V		63	126		185		160	ns
			4.5 V		13	25		37		32	
			6 V		11	21		32		27	
t <sub>t</sub>			2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C <sub>pd</sub>	Power dissipation capacitance per flip-flop	No load, T <sub>A</sub> = 25°C	30 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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