

TC74HC7292P TC74HC7294P

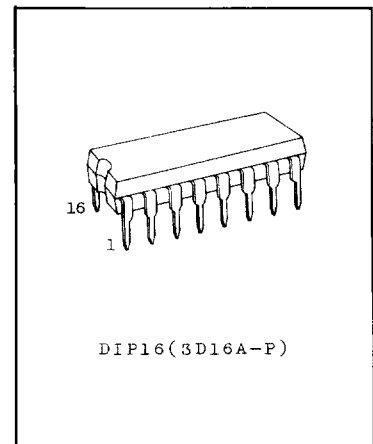
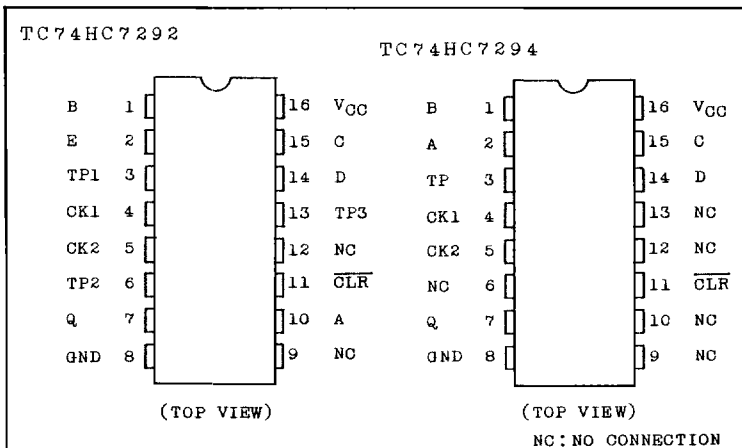
TC74HC7292P PROGRAMMABLE DIVIDER/TIMER
TC74HC7294P PROGRAMMABLE DIVIDER/TIMER

The TC74HC7292 and TC74HC7294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These devices are programmable frequency divider. Both types have two clock inputs, either one may be used for clock gating. (See the function table (1)). The TC74HC7292 can divide from 2² to 2³¹, and the TC74HC7294 can divide from 2² to 2¹⁵. Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the 74HC7292 and TP on the 74HC7294). All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed $f_{MAX} = \begin{matrix} 50\text{MHz} & [7292] \\ 60\text{MHz} & [7294] \end{matrix}$ (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation $I_{CC} = 4\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability 10 LSTTL Loads
- Summetrical Output Impedance $|I_{OH}| = I_{OL} = 4mA$ (Min.)
- Balanced Propagation Delays $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range..... $V_{CC}(\text{Opr.}) = 2V \sim 6V$
- Pin and Function Compatible with 74LS292/294

PIN ASSIGNMENT



TC74HC7292P TC74HC7294P

TRUTH TABLE

CLEAR	CLOCK 1	CLOCK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H		L	UP Count
H	L		
H	H	X	NO Change
H	X	H	

TC74HC7292

PROGRAMMING INPUTS	FREQUENCY DIVISION							
	Q		TP1		TP2		TP2	
E D C B A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L L L L L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L L L L H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L L L H -L	2 ²	4	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L L L H H	2 ³	8	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L L H L L	2 ⁴	16	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L L H L H	2 ⁵	32	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L L H H L	2 ⁶	64	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L L H H H	2 ⁷	128	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
L H L L L	2 ⁸	256	2 ⁹	512	2 ¹⁷	131,072	2 ²	4
L H L L H	2 ⁹	512	2 ⁹	512	2 ¹⁷	131,072	2 ²	4
L H L H L	2 ¹⁰	1,024	2 ⁹	512	2 ¹⁷	131,072	2 ⁴	16
L H L H H	2 ¹¹	2,048	2 ⁹	512	2 ¹⁷	131,072	2 ⁴	16
L H H L L	2 ¹²	4,096	2 ⁹	512	2 ¹⁷	131,072	2 ⁶	64
L H H L H	2 ¹³	8,192	2 ⁹	512	2 ¹⁷	131,072	2 ⁶	64
L H H H L	2 ¹⁴	16,384	2 ⁹	512	Disabled Low		2 ⁸	256
L H H H H	2 ¹⁵	32,768	2 ⁹	512	Disabled Low		2 ⁸	256
H L L L L	2 ¹⁶	65,536	2 ⁹	512	2 ³	8	2 ¹⁰	1,024
H L L L H	2 ¹⁷	131,072	2 ⁹	512	2 ³	8	2 ¹⁰	1,024
H L L H L	2 ¹⁸	262,144	2 ⁹	512	2 ⁵	32	2 ¹²	4,096
H L L H H	2 ¹⁹	524,288	2 ⁹	512	2 ⁵	32	2 ¹²	4,096
H L H L L	2 ²⁰	1,048,576	2 ⁹	512	2 ⁷	128	2 ¹⁴	16,384
H L H L H	2 ²¹	2,097,152	2 ⁹	512	2 ⁷	128	2 ¹⁴	16,384
H L H H L	2 ²²	4,194,304	Disabled Low		2 ⁹	512	2 ¹⁶	65,536
H L H H H	2 ²³	8,388,608	Disabled Low		2 ⁹	512	2 ¹⁶	65,536
H H L L L	2 ²⁴	16,777,216	2 ³	8	2 ¹¹	2,048	2 ¹⁸	262,144
H H L L H	2 ²⁵	33,554,432	2 ³	8	2 ¹¹	2,048	2 ¹⁸	262,144
H H L H L	2 ²⁶	67,108,864	2 ⁵	32	2 ¹³	8,192	2 ²⁰	1,048,576
H H L H H	2 ²⁷	134,217,728	2 ⁵	32	2 ¹³	8,192	2 ²⁰	1,048,576
H H H L L	2 ²⁸	268,435,456	2 ⁷	128	2 ¹⁵	32,768	2 ²²	4,194,304
H H H L H	2 ²⁹	536,870,912	2 ⁷	128	2 ¹⁵	32,768	2 ²²	4,194,304
H H H H L	2 ³⁰	1,073,741,824	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216
H H H H H	2 ³¹	2,147,483,648	2 ⁹	512	2 ¹⁷	131,072	2 ²⁴	16,777,216

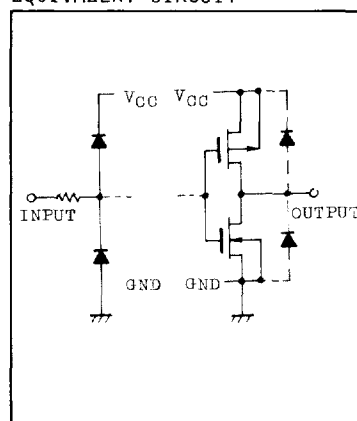
TRUTH TABLE

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2 ²	4	2 ⁹	512
L	L	H	H	2 ³	8	2 ⁹	512
L	H	L	L	2 ⁴	16	2 ⁹	512
L	H	L	H	2 ⁵	32	2 ⁹	512
L	H	H	L	2 ⁶	64	2 ⁹	512
L	H	H	H	2 ⁷	128	Disabled Low	
H	L	L	L	2 ⁸	256	2 ²	4
H	L	L	H	2 ⁹	512	2 ³	8
H	L	H	L	2 ¹⁰	1,024	2 ⁴	16
H	L	H	H	2 ¹¹	2,048	2 ⁵	32
H	H	L	L	2 ¹²	4,096	2 ⁶	64
H	H	L	H	2 ¹³	8,192	2 ⁷	128
H	H	H	L	2 ¹⁴	16,384	2 ⁸	256
H	H	H	H	2 ¹⁵	32,768	2 ⁹	512

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	-0.5 ~ 7	V
DC Input Voltage	V _{IN}	-0.5 ~ V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5 ~ V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	+20	mA
DC Output Current	I _{OUT}	+25	mA
DC V _{CC} /Ground Current	I _{CC}	±50	mA
Power Dissipation	P _D	500*	mW
Storage Temperature	T _{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T _L	300	°C

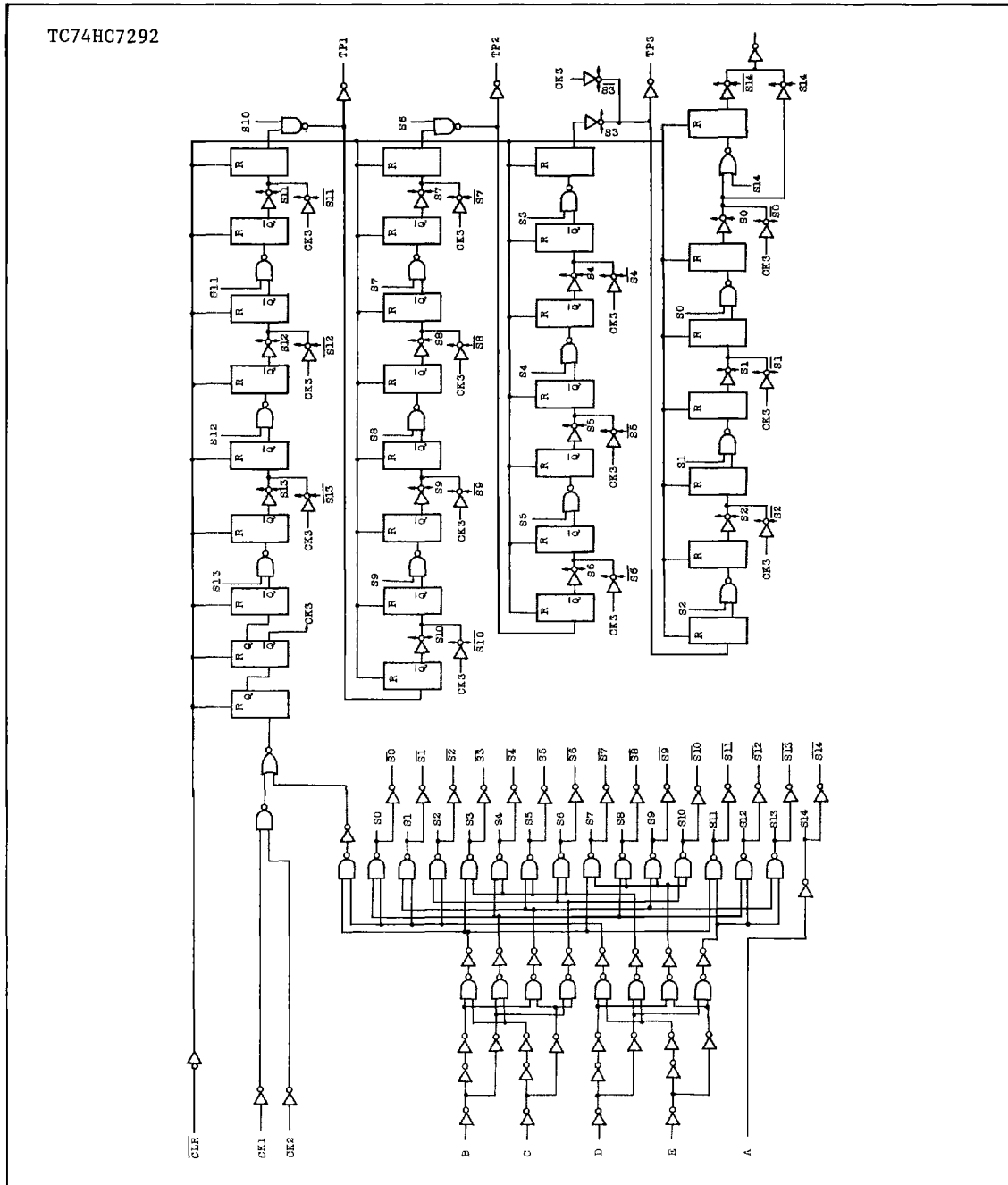
INPUT and OUTPUT EQUIVALENT CIRCUIT



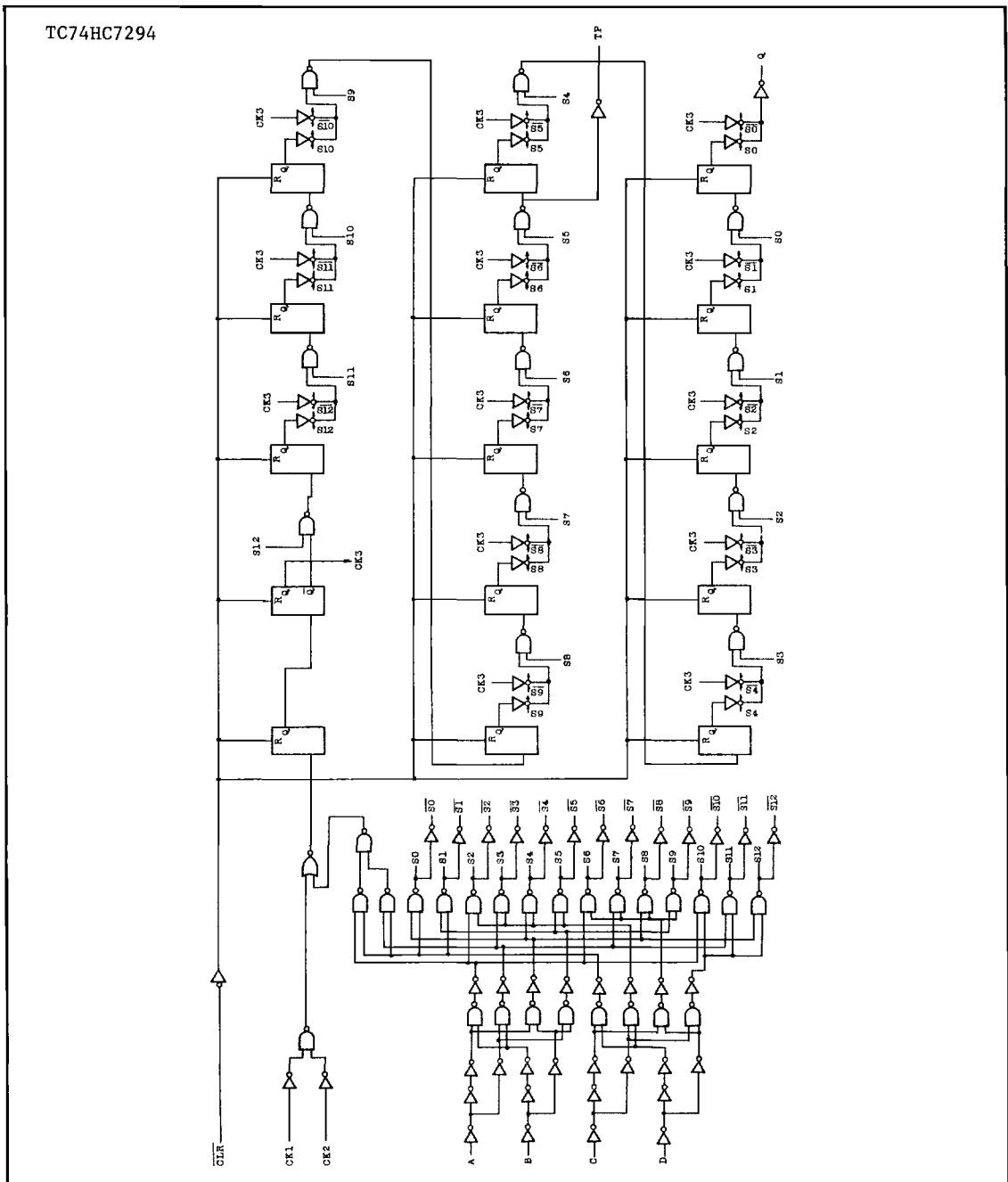
* 500mW in the range of T_a=-40°C ~ 65°C and from T_a=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

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LOGIC DIAGRAM



LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	
Output Voltage	V_{OUT}	0 ~ V_{CC}	
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 ($V_{CC}=2.0V$) 0 ~ 500 ($V_{CC}=4.5V$) 0 ~ 400 ($V_{CC}=6.0V$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	$T_a=25^\circ C$			$T_a=-40\sim 85^\circ C$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V	
			4.5	3.15	-	-	3.15	-		
			6.0	4.2	-	-	4.2	-		
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V	
			4.5	-	-	1.35	-	1.35		
			6.0	-	-	1.8	-	1.8		
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	V
				6.0	5.68	5.80	-	5.63	-	
				6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	V
				6.0	-	0.18	0.26	-	0.33	
				6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	± 0.1	-	± 1.0	μA	
			6.0	-	-	4.0	-	40.0		
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	4.0	-	40.0	μA	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6\text{ns}$, $C_L=50\text{pF}$)

PARAMETER	SYMBOL	TEST CONDITION	VCC	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q)	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Transition Time (TP)	t_{TLH}		2.0	-	132	255	-	320	
	t_{THL}		4.5	-	33	51	-	64	
			6.0	-	28	43	-	54	
Propagation Delay Time (CLOCK - Q) *	t_{pLH}	B="H"	2.0	-	264	500	-	625	
	t_{pHL}	A=C=D=E="L"	4.5	-	66	100	-	125	
			6.0	-	56	85	-	106	
Propagation Delay Time (CLOCK - Q) **	t_{pLH}	B="H"	2.0	-	236	455	-	570	
	t_{pHL}	A=C=D="L"	4.5	-	59	91	-	114	
			6.0	-	50	77	-	97	
Propagation Delay Time ($\overline{\text{CLEAR}}$ - Q) *	t_{pHL}		2.0	-	224	425	-	530	
			4.5	-	56	85	-	106	
			6.0	-	48	72	-	90	
Propagation Delay Time ($\overline{\text{CLEAR}}$ - Q) **	t_{pHL}		2.0	-	204	390	-	490	
			4.5	-	51	78	-	98	
			6.0	-	43	66	-	83	
* Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	32	48	-	26	-	
			6.0	38	56	-	31	-	
** Maximum Clock Frequency	f_{MAX}		2.0	7	14	-	6	-	
			4.5	32	55	-	30	-	
			6.0	44	65	-	35	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$		2.0	-	36	100	-	125	ns
	$t_{w(L)}$		4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Pulse Width ($\overline{\text{CLEAR}}$) *	$t_{w(L)}$		2.0	-	60	150	-	190	
			4.5	-	15	30	-	38	
			6.0	-	13	26	-	32	
Minimum Pulse Width ($\overline{\text{CLEAR}}$) **	$t_{w(L)}$		2.0	-	72	175	-	220	
			4.5	-	18	35	-	44	
			6.0	-	15	30	-	37	
Minimum Removal Time ($\overline{\text{CLEAR}}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$	74HC7292		-	22	-	-	-	
		74HC7294		-	23	-	-	-	

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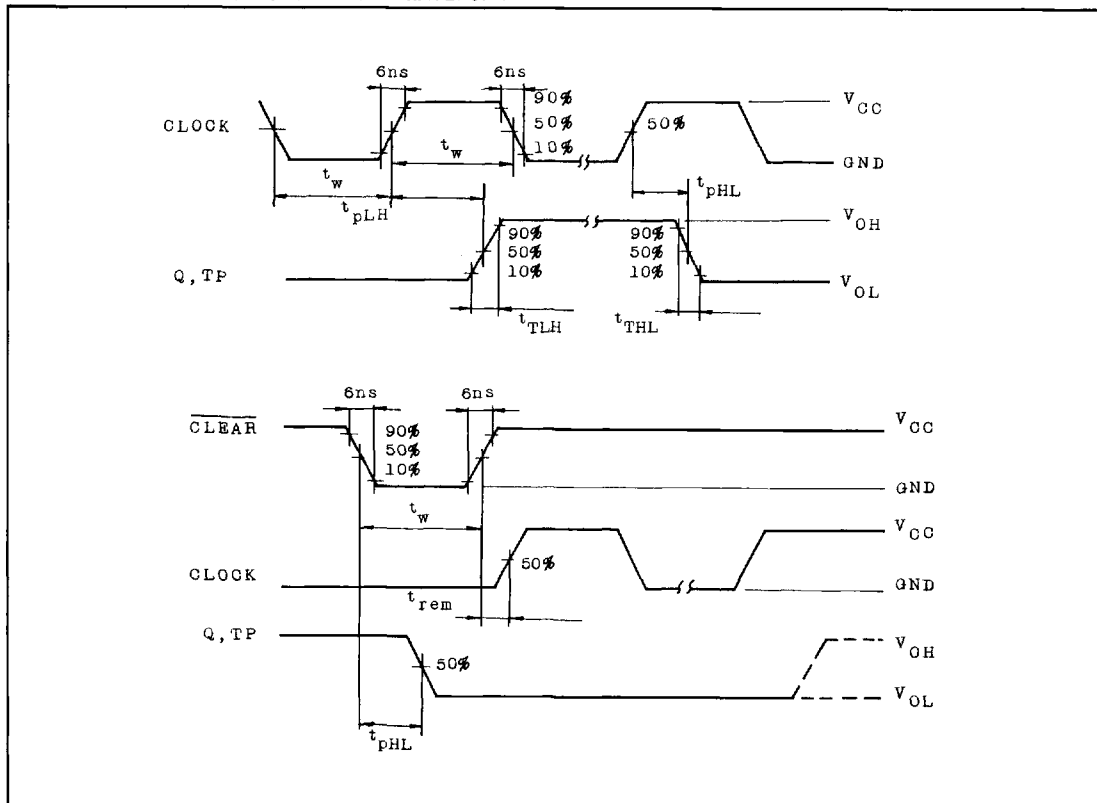
Note(1): C_{pd} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(\text{Opr.}) = C_{pd} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

(2): * ; for TC74HC7292

** ; for TC74HC7294

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC}(\text{Opr.})$ TEST CIRCUIT

