TC74HC696AP/AF•TC74HC697AP/AF
TC74HC698AP/AF•TC74HC699AP/AF

SYNCHRONOUS PRESETTABLE 4-BIT UP/DOWN COUNTER WITH OUTPUT REGISTER (MULTIPLEXED 3-STATE OUTPUTS)

TC74HC696AP/AF DECADE, ASYNCHRONOUS CLEAR
TC74HC697AP/AF BINARY, ASYNCHRONOUS CLEAR
TC74HC698AP/AF DECADE, SYNCHRONOUS CLEAR
TC74HC699AP/AF BINARY, SYNCHRONOUS CLEAR

The TC74HC696A, 697A, 698A, and 699A are high speed CMOS UP/DOWN COUNTERS fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC696A/698A are BCD decade counters and the TC74HC679A/699A are 4 bit binary counters.

They count on the rising edge of the Counter Clock (CCK) input when "counter mode" is selected. If the up/down ($U/\overline{D}$) input is held high, the internal counter counts up. Conversely, if $U/\overline{D}$ is held low, it counts down. The internal counters' outputs are latched into the output registers on the rising edge of the Register Clock (RCK) input.

The outputs (QA~QD) are selected as either internal counter or registered outputs by the output select ($R/\overline{C}$) input. When high, the outputs are counter outputs and when low, they are registered outputs.

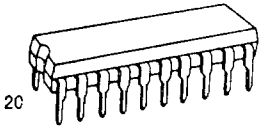
The clear function of the TC74HC698A/699A are synchronous to clock, while the TC74HC696A/697A are cleared asynchronously.

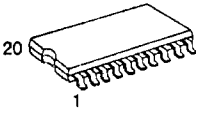
Two enable ($\overline{ENP}$, $\overline{ENT}$) inputs and a carry ($\overline{RCO}$) output are provided to enable cascading of the counters. This facilitates easy implementation of n-bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

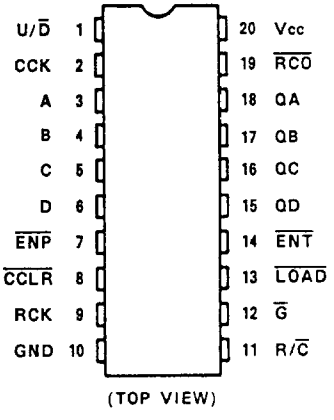
FEATURES:

- High Speed ····· f_{MAX}=38MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For Q_A~Q_D
  10 LSTTL Loads For $\overline{RCO}$
- Symmetrical Output Impedance·····$|I_{OH}|=I_{OL}$=6mA(Min.) For Q_A~Q_D
  $|I_{OH}|=I_{OL}$=4mA(Min.) For $\overline{RCO}$
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS696~699





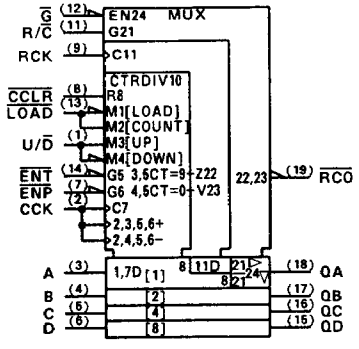
PIN ASSIGNMENT



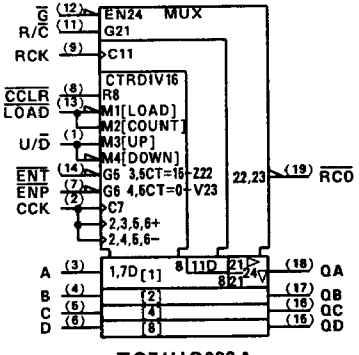
(TOP VIEW)

IEC LOGIC SYMBOL

TC74HC696A



TC74HC697A



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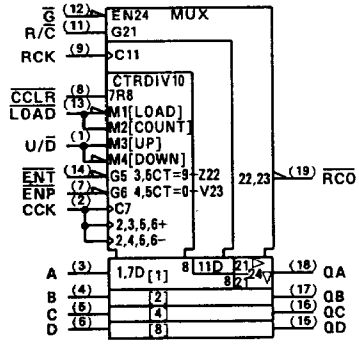
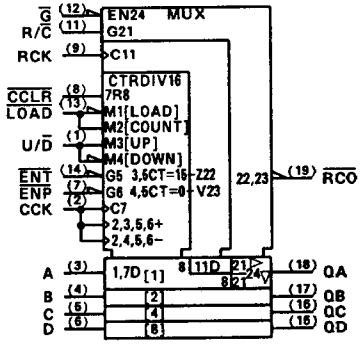


TC74HC699A



TRUTH TABLE

INPUTS										OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	*CCK	**CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	CD	
X	X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH INPEDANCE
L	X	X	X	X	↓	X	X	L	L	L	L	L	L	CREAR COUNTER
H	L	X	X	↓	↓	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↓	↓	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↓	↓	X	X	L	L					
H	H	L	L	↓	↓	H	X	L	L	COUNT UP				COUNT
H	H	L	L	↓	↓	L	X	L	L	COUNT DOWN				COUNT
H	X	X	X	↑	↑	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	X	↓	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	X	↑	H	L	NO CHANGE				NO COUNT

X : Don't care

Z : High Impedance

• TC74HC696A/697A

• • TC74HC698A/699A

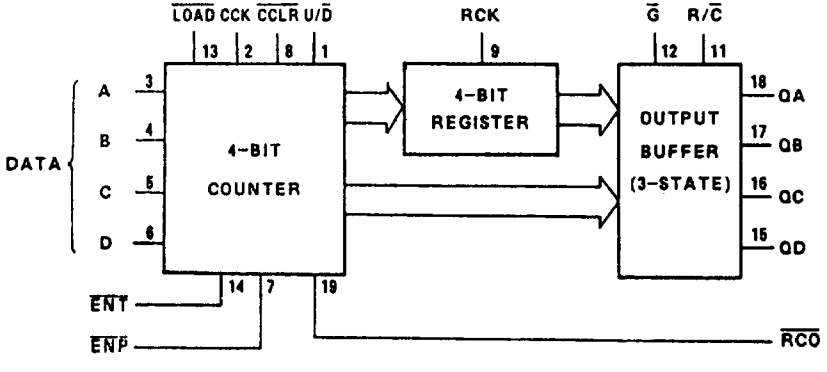
a ~ d : The level of steady state inputs at inputs A through D respectively.

a' ~ d' : The level of steady state outputs at internal counter outputs QA' through QD' respectively.

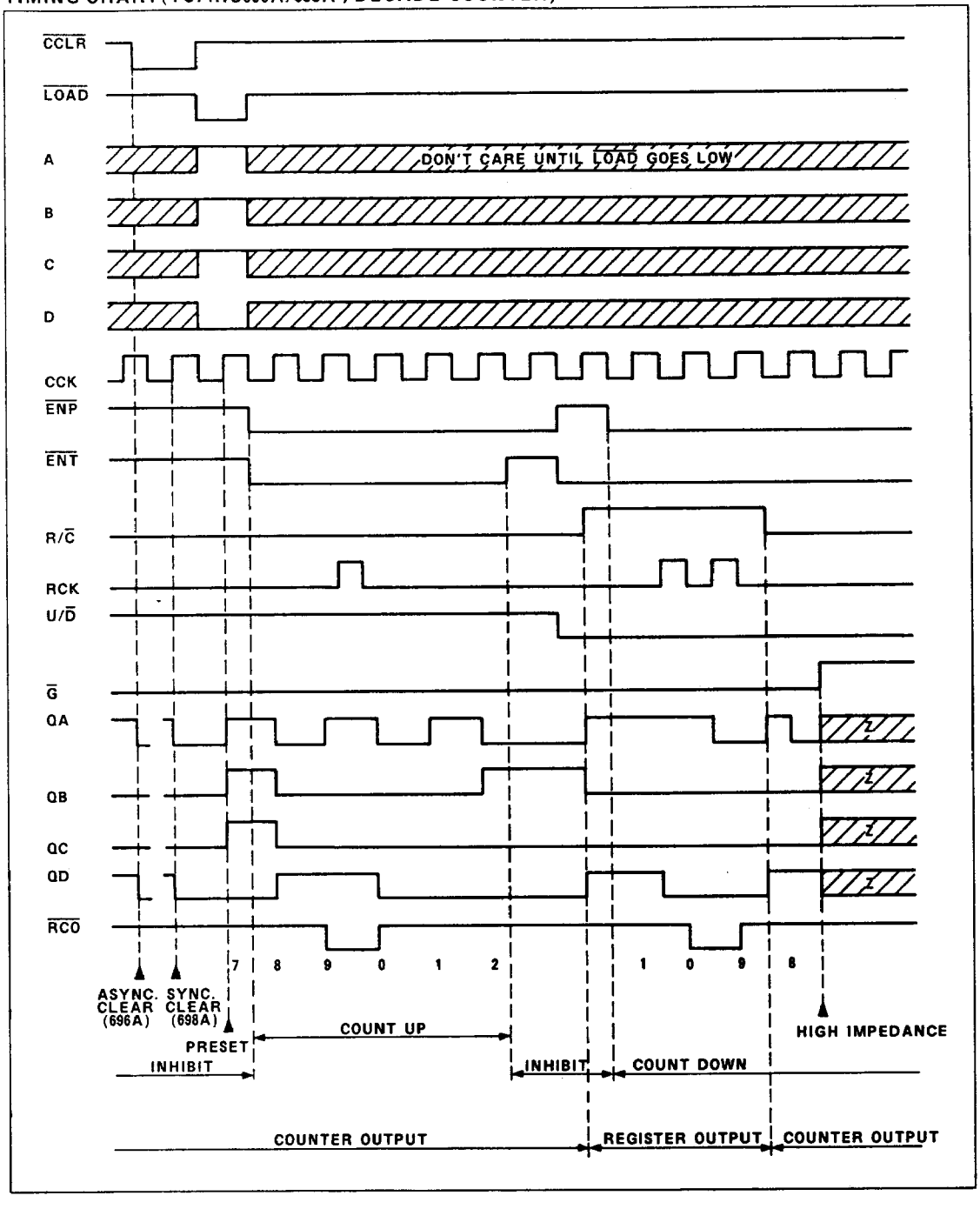
HC696A/698A ; $\overline{RCO}=(\overline{UP \cdot QA \cdot QD \cdot ENT + UP \cdot \overline{QA} \cdot \overline{QD} \cdot ENT})$

HC697A/699A ; $\overline{RCO}=(\overline{UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + UP \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT})$

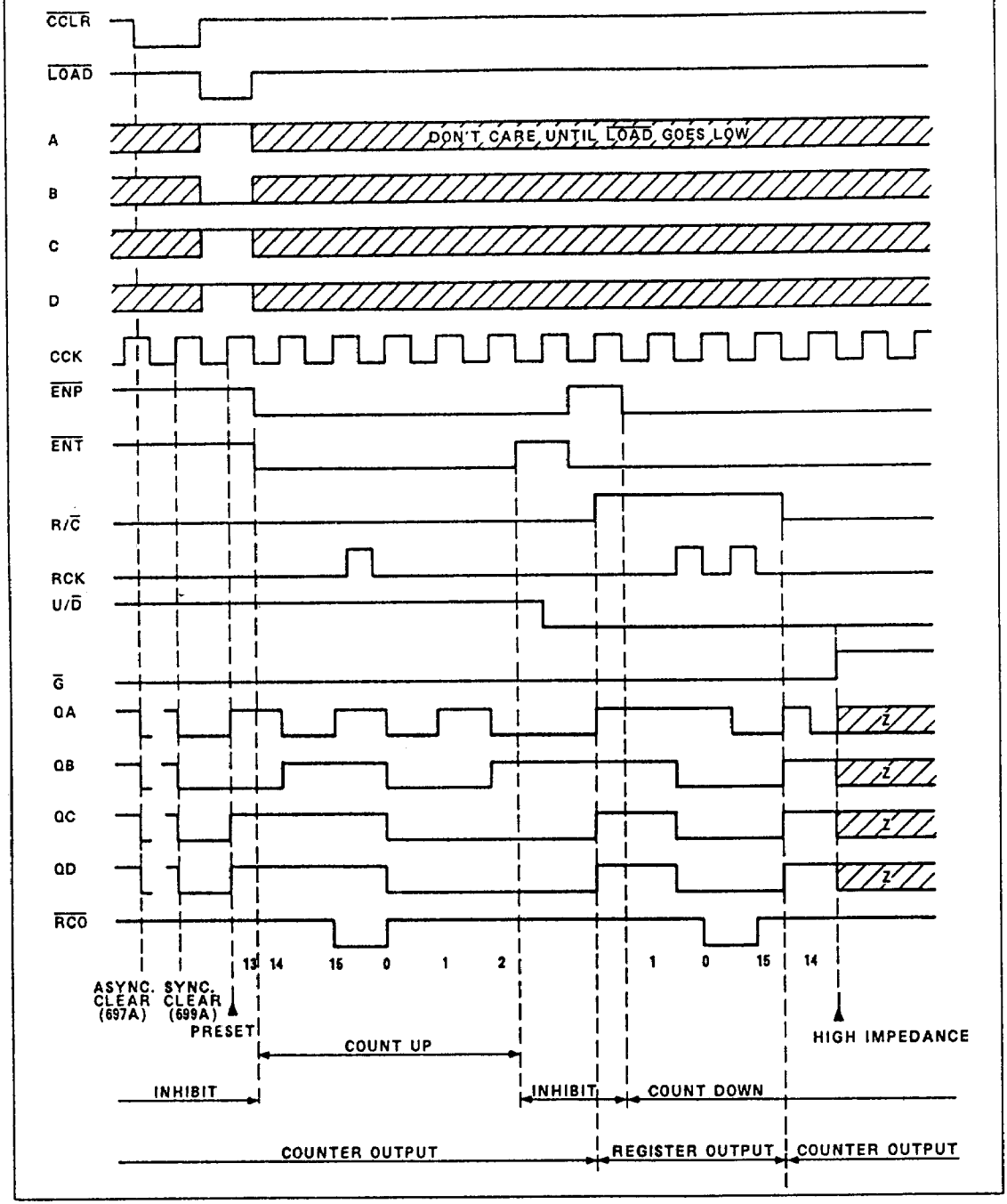
BLOCK DIAGRAM



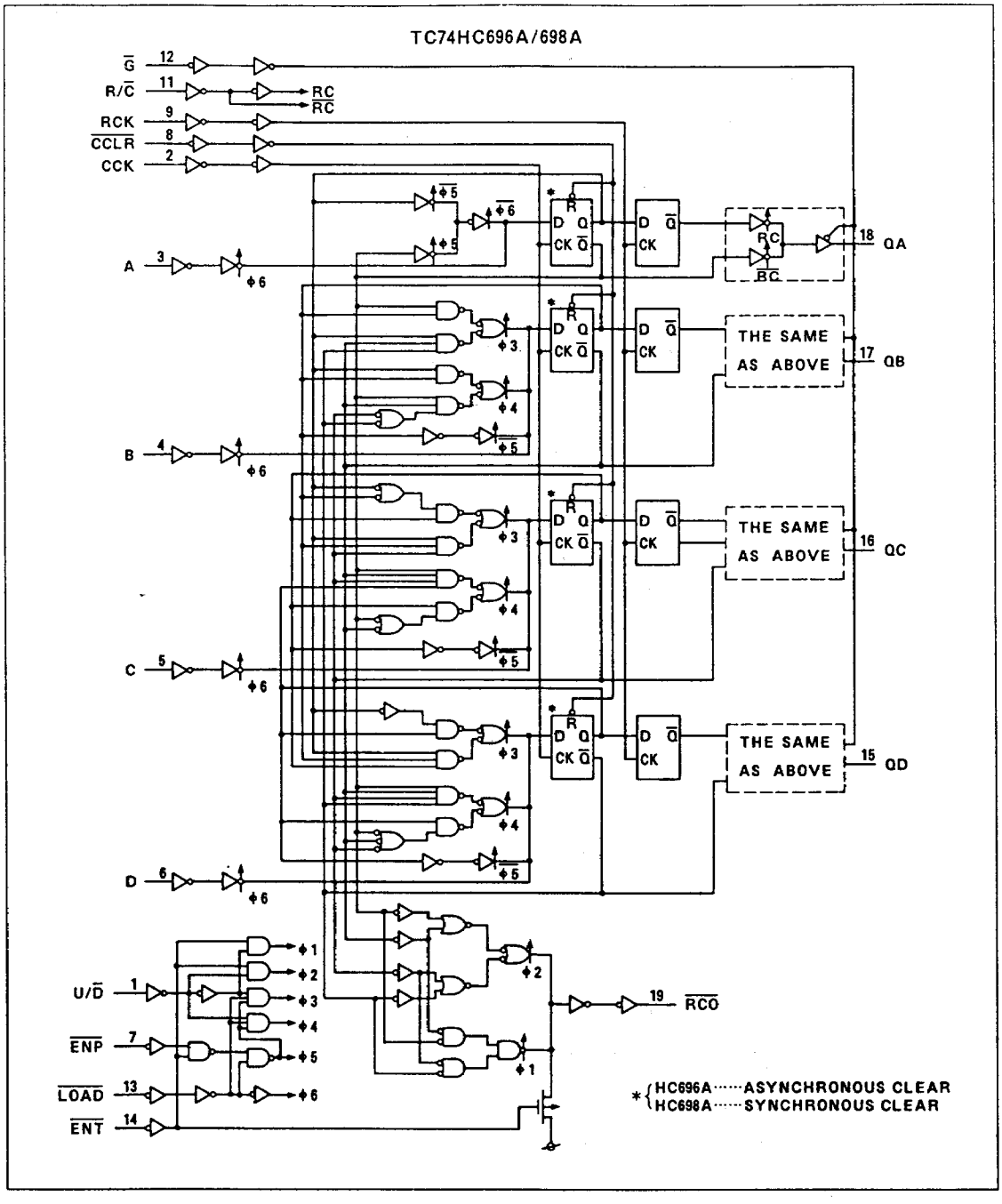
TIMING CHART(TC74HC696A/698A ; DECADE COUNTER)



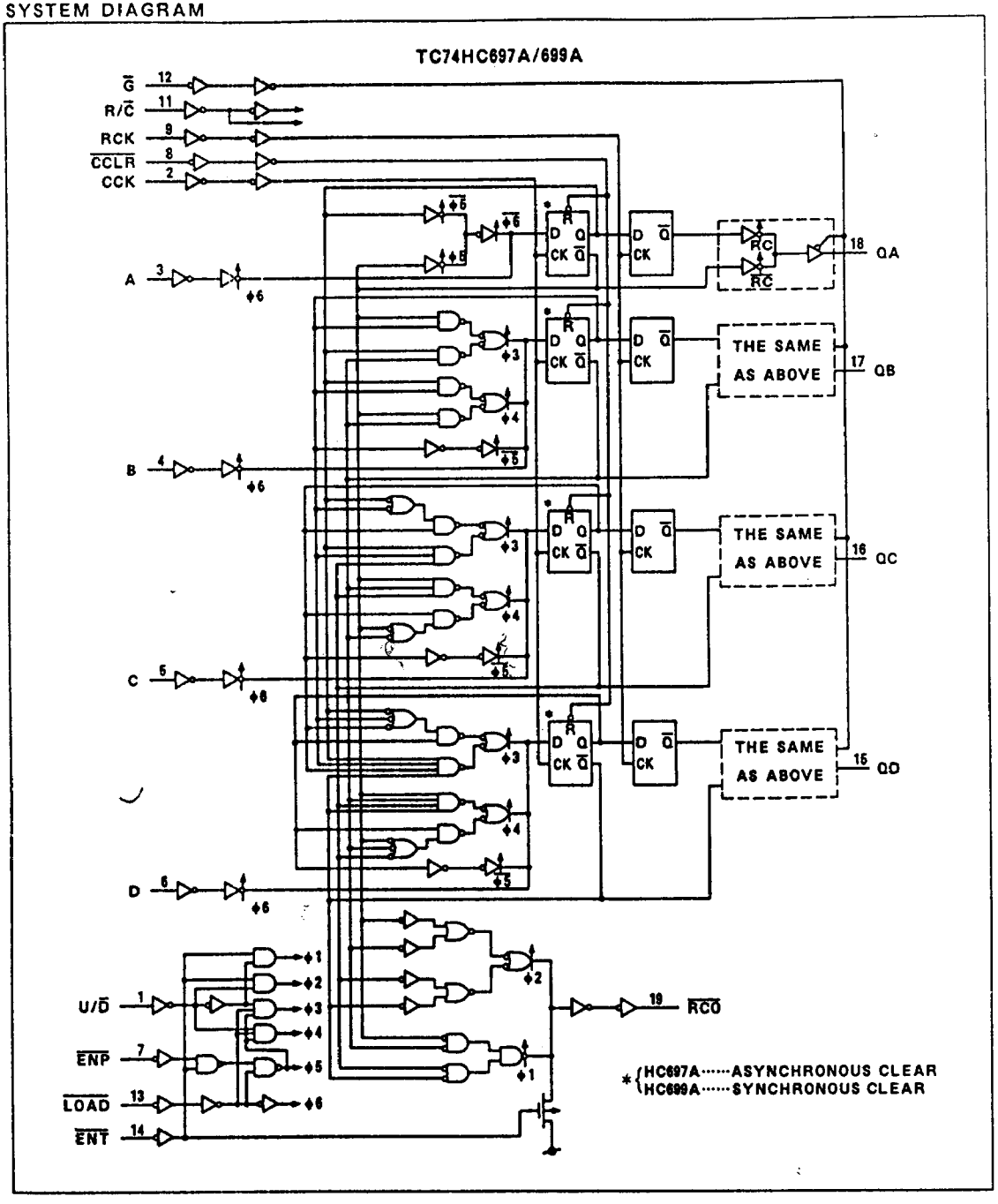
TIMING CHART (TC74HC697A/699A ; BINARY COUNTER)



SYSTEM DIAGRAM



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current $\frac{(\overline{RCO})}{(Q_A \sim Q_D)}$	I_{OUT}	± 25 ± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		$\overline{RCO}$	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
		$Q_A \sim Q_D$	I_{OH} =−6 mA	4.5	4.18	4.31	−	4.31	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		$\overline{RCO}$	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
		$Q_A \sim Q_D$	I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C		Ta=−40 ~85°C	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CCK, RCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CCLR}$)*	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($\overline{CCLR}$)**	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set−up Time ($\overline{LOAD}$, $\overline{ENT}$, $\overline{ENP}$)	t_s		2.0	−	150	190	
			4.5	−	30	38	
			6.0	−	13	32	
Minimum Set−up Time (A, B, C, D)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set−up Time (U/$\overline{D}$)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (CCK−RCK)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Hold Time (A, B, C, D)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Hold Time ($\overline{CCLR}$)**	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time *	t_{rem}		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	5	4	MHz
			4.5	−	25	20	
			6.0	−	29	24	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		−	4	8	ns
Output Transition Time (CCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		−	24	41	
Propagation Delay Time (ENT−$\overline{RCO}$)	t_{pLH} t_{pHL}		−	13	23	
Propagation Delay Time ($\overline{CCLR}$−$\overline{RCO}$)*	t_{pLH} t_{pHL}		−	23	38	
Maximum Clock Frequency	f_{MAX}		25	38	−	MHz

* : for TC74HC696A/697A only
** : for TC74HC698A/699A only

AC ELECTRICAL CHARACTERISTICS(Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		50	2.0	−	30	75	−	95	
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (CCK−Q)	t_{pLH} t_{pHL}		50	2.0	−	90	195	−	245	
				4.5	−	26	39	−	49	
				6.0	−	19	33	−	42	
			150	2.0	−	103	235	−	295	
				4.5	−	31	47	−	59	
				6.0	−	23	40	−	50	
Propagation Delay Time (RCK−Q)	t_{pLH} t_{pHL}		50	2.0	−	82	180	−	225	
				4.5	−	24	36	−	45	
				6.0	−	18	31	−	38	
			150	2.0	−	95	220	−	275	
				4.5	−	29	44	−	55	
				6.0	−	22	37	−	47	
Propagation Delay Time (R/$\overline{C}$−Q)	t_{pLH} t_{pHL}		50	2.0	−	60	145	−	180	
				4.5	−	19	29	−	36	
				6.0	−	14	25	−	31	
			150	2.0	−	73	185	−	230	
				4.5	−	24	37	−	46	
				6.0	−	18	31	−	39	
Propagation Delay Time ($\overline{CCLR}$−Q)*	t_{pHL}		50	2.0	−	89	195	−	245	
				4.5	−	26	39	−	49	
				6.0	−	20	33	−	42	
			150	2.0	−	102	235	−	295	
				4.5	−	31	47	−	59	
				6.0	−	24	40	−	50	
Propagation Delay Time (CCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		50	2.0	−	108	235	−	295	
				4.5	−	31	47	−	59	
				6.0	−	23	40	−	50	
Propagation Delay Time ($\overline{ENT}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		50	2.0	−	63	135	−	170	
				4.5	−	18	27	−	34	
				6.0	−	14	23	−	29	
Propagation Delay Time ($\overline{CCLR}$−$\overline{RCO}$)*	t_{pLH} t_{pHL}		50	2.0	−	98	220	−	275	
				4.5	−	29	44	−	55	
				6.0	−	23	37	−	47	

* for TC74HC696A/697A only

AC ELECTRICAL CHARACTERISTICS(Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Enable time ($\overline{G}$–Q)*	t_{pZL} t_{pZH}	$R_L = 1\,k\Omega$	50	2.0	–	45	115	–	145	ns
				4.5	–	15	23	–	29	
				6.0	–	12	20	–	25	
			150	2.0	–	58	155	–	195	
				4.5	–	20	31	–	39	
				6.0	–	16	26	–	33	
Output Enable time ($\overline{G}$–Q)**	t_{pZL} t_{pZH}	$R_L = 1\,k\Omega$	50	2.0	–	46	110	–	140	
				4.5	–	14	22	–	28	
				6.0	–	12	19	–	24	
			150	2.0	–	62	150	–	190	
				4.5	–	19	30	–	38	
				6.0	–	16	26	–	33	
Output Disable time ($\overline{G}$–Q)	t_{pLZ} t_{pHZ}	$R_L = 1\,k\Omega$	50	2.0	–	32	115	–	145	
				4.5	–	17	23	–	29	
				6.0	–	14	20	–	25	
Maximum Clock Frequency	f_{MAX}		50	2.0	5	11	–	4	–	
				4.5	25	38	–	20	–	
				6.0	29	52	–	24	–	
Input Capacitance	C_{IN}				–	5	10	–	10	pF
Output Capacitance	C_{OUT}				–	13	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)				–	72	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Note (2) * : for TC74HC696A/697A only
** : for TC74HC698A/699A only