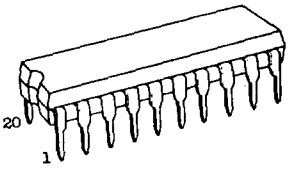
TC74HC698P
TC74HC699P

TC74HC698P U/D DECADE COUNTER/REGISTER (3-STATE)
TC74HC699P U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

The TC74HC698/699 are high speed CMOS up/down counters fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. TC74HC698 is BCD DECADE COUNTER, and TC74HC699 is 4-BIT BINARY COUNTER. Both devices have registers respectively. They count at positive edge of counter clock input (CCK) when selected at "Counter Mode". If input U/$\overline{D}$ is held "H", internal counter counts up, and held "L", counts down. Internal counter's outputs are memoried in output register at positive edge of register clock (RCK). The outputs (QA ∿ QD) are selected internal counter outputs or register outputs respectively by output select input (R/$\overline{C}$). Their clear function are cleared synchronously to clock. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=31MHz(Max.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads (For $\overline{RCO}$)
  15 LSTTL Loads (For QA ∿ QD)
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA ∿ QD Output
  $|I_{OH}|=I_{OL}$=4mA(Min.)For $\overline{RCO}$ Output
- Balanced Propagation Delays ..... $t_{pLH} \doteq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL (74LS698/699)



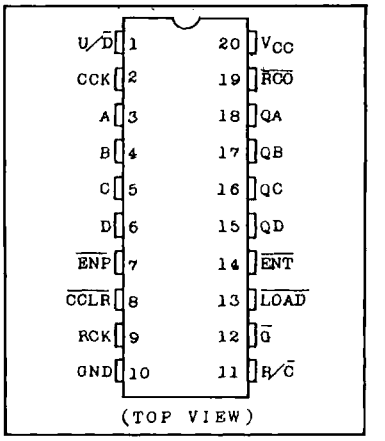
DIP20(3D20AP)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35 (QA ∿ QD) ±25 ($\overline{RCO}$)	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10 sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIBNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	↓	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↓	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↓	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↓	X	X	L	L					
H	H	L	L	↓	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↓	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	↑	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↓	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↑	H	L	NO CHANGE				NO LOAD

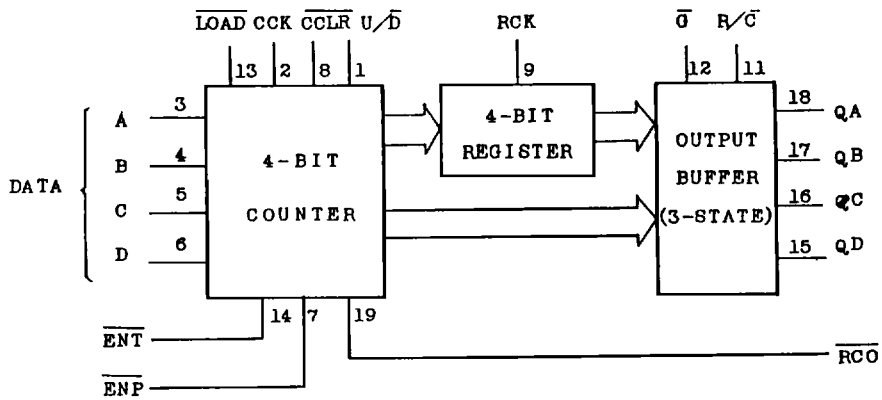
X: Don't care
Z: High Impedance
a ∿ d : The level of steady state inputs at inputs A through D respectively.
a' ∿ d': The level of steady state outputs at internal counter outputs QA' through QD' respectively.

$\overline{RCO}$ Function

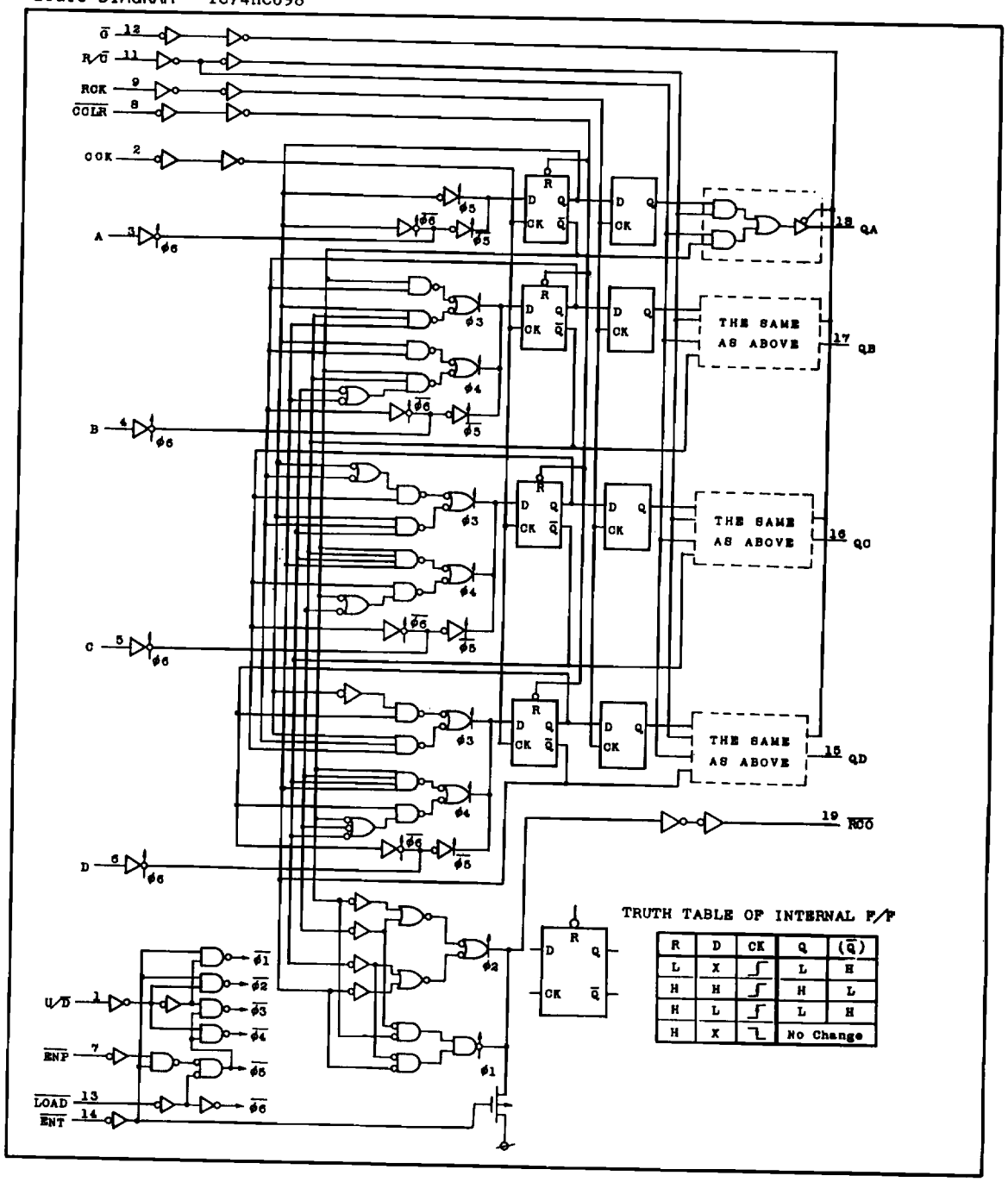
TC74HC698 $\overline{RCO}=\overline{(UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QD} \cdot ENT)}$

TC74HC699 $\overline{RCO}=\overline{(UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT)}$

BLOCK DIAGRAM

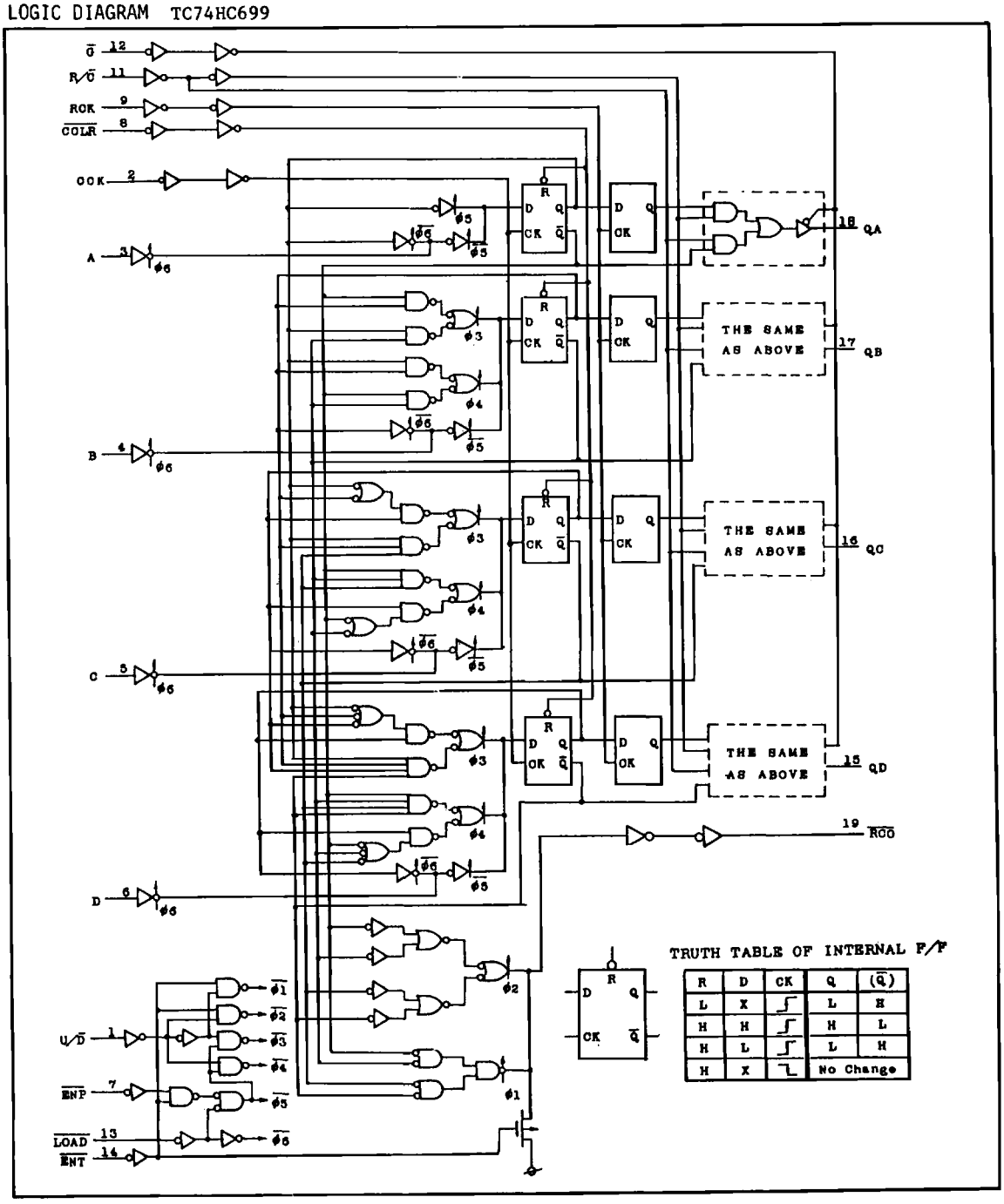


LOGIC DIAGRAM TC74HC698



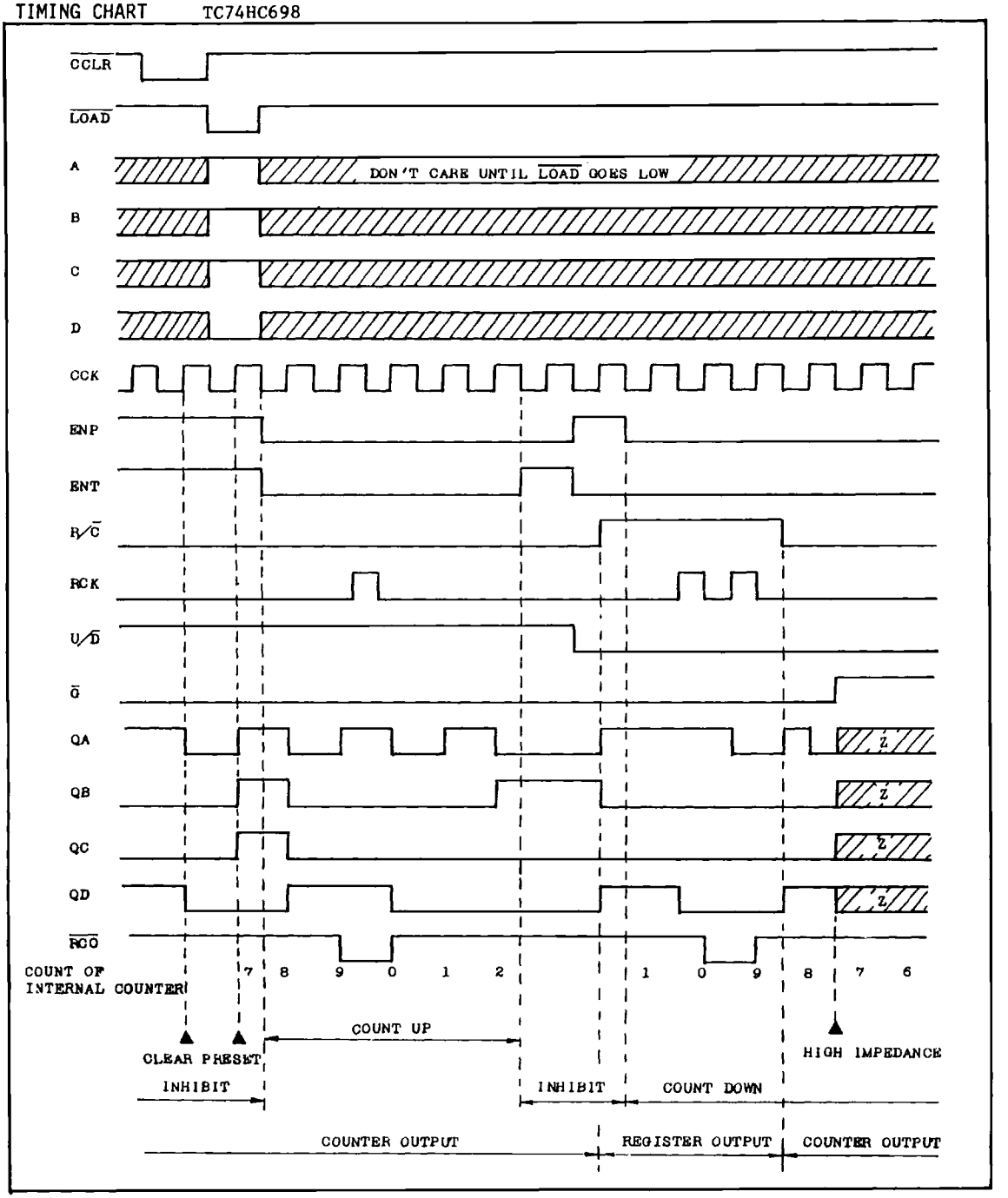
R	D	CK	Q	(Q̄)
L	X	↓	L	H
H	H	↓	H	L
H	L	↓	L	H
H	X	↑	No Change	

LOGIC DIAGRAM TC74HC699

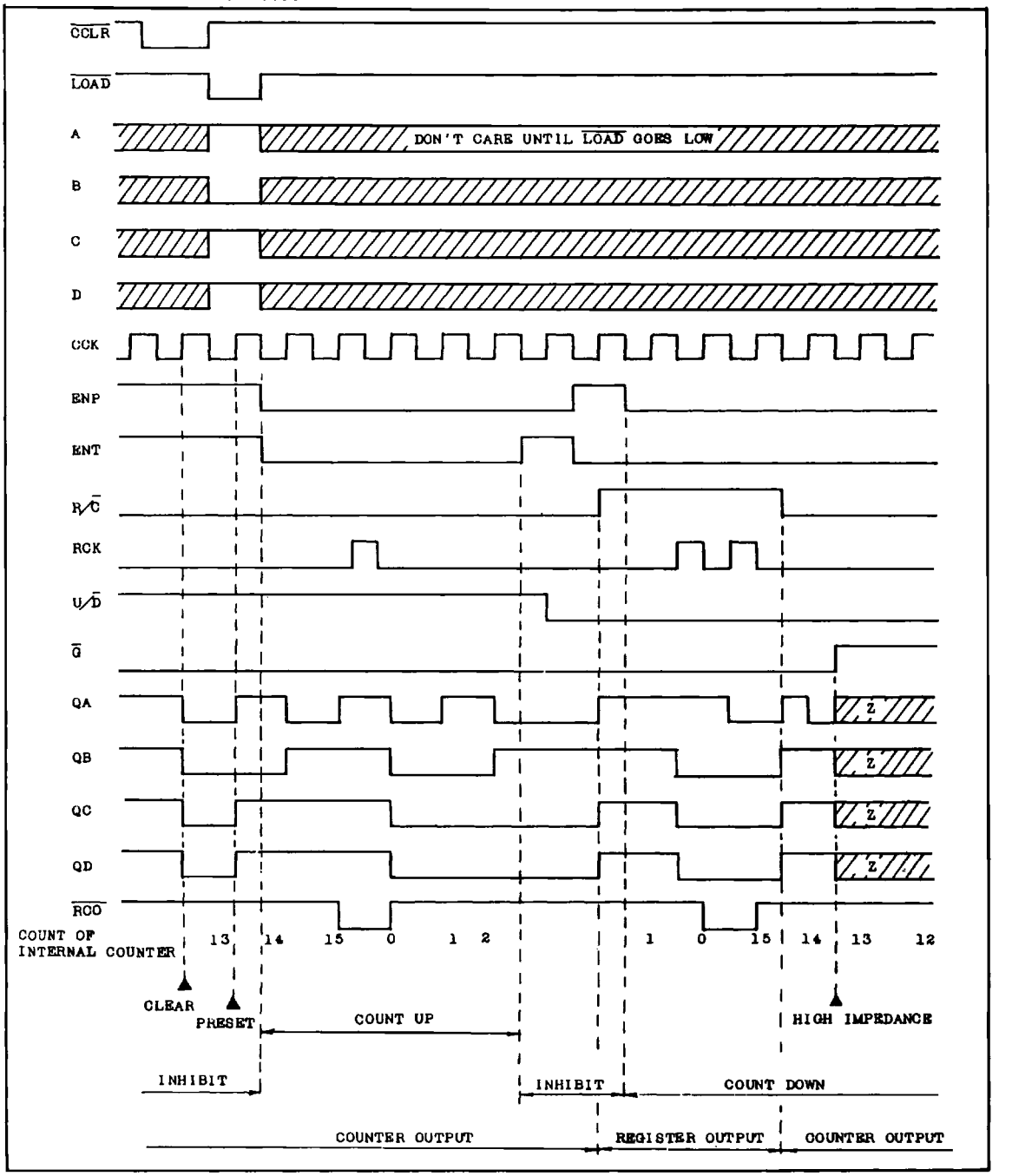


R	D	CK	Q	$\overline{Q}$
L	X	↓	L	H
H	H	↓	H	L
H	L	↓	L	H
H	X	↑	No Change	

TIMING CHART TC74HC698



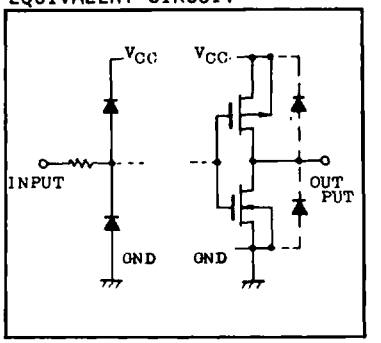
TIMING CHART TC74HC699



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40∿85°C MIN.	Ta=−40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		QA ∿ QD	I_{OH}=−6mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−7.8mA	6.0	5.68	5.80	−	5.63	−	
		$\overline{RCO}$	I_{OH}=−4mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		QA ∿ QD	I_{OL}=6mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=7.8mA	6.0	−	0.18	0.26	−	0.33	
		$\overline{RCO}$	I_{OL}=4mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{OUT}=V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	144	275	-	345	
			4.5	-	36	55	-	69	
			6.0	-	31	47	-	59	
Propagation Delay Time (R/$\overline{C}$ - Q)	t_{pLH} t_{pHL}		2.0	-	92	175	-	220	
			4.5	-	23	35	-	44	
			6.0	-	20	30	-	37	
Propagation Delay Time ($\overline{ENT}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	96	190	-	240	
			4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	
Maximum Clock Frequency (CCK, RCK)	f_{MAX}		2.0	3.5	7	-	2.5	-	MHz
			4.5	18	28	-	14	-	
			6.0	21	33	-	16	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	44	100	-	125	ns
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time ($\overline{LOAD}$, $\overline{ENP}$, $\overline{ENT}$)	t_s		2.0	-	84	200	-	250	
			4.5	-	21	40	-	50	
			6.0	-	18	34	-	43	
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	16	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	

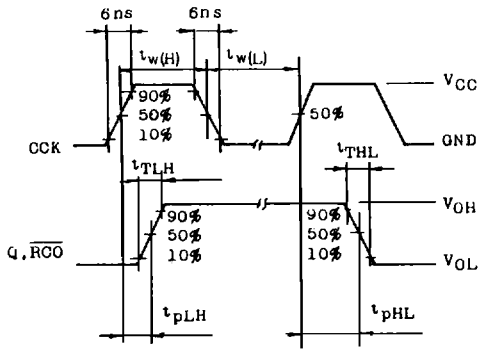
AC ELECTRICAL CHARACTERISTICS (Continued)

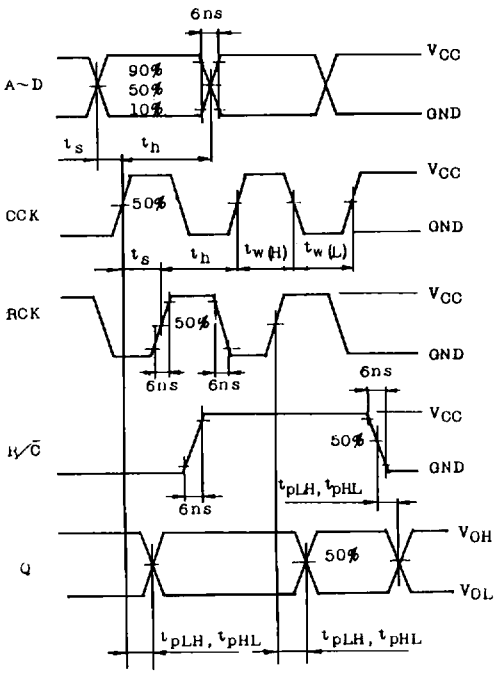
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Set-up Time ($\overline{CCLR}$)	t_s		2.0	-	12	50	-	65	ns
			4.5	-	3	10	-	13	
			6.0	-	2.5	9	-	11	
Minimum Set-up Time (U/$\overline{D}$)	t_s		2.0	-	60	150	-	190	
			4.5	-	15	30	-	38	
			6.0	-	13	26	-	32	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Hold Time	t_h		2.0	-	-	25	-	36	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	80	145	-	180	
			4.5	-	20	29	-	36	
			6.0	-	17	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD} (1)			-	113	-	-	-	

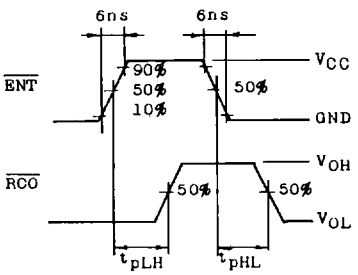
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

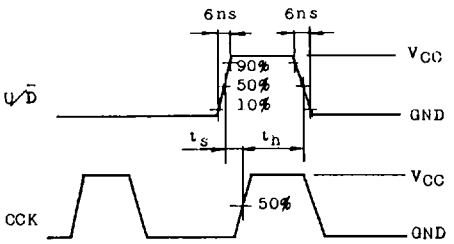
$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

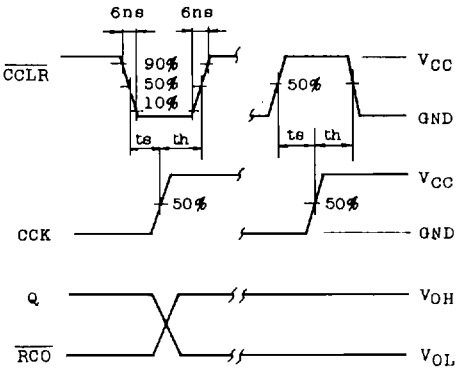
SWITCHING CHARACTERISTICS TEST WAVEFORM



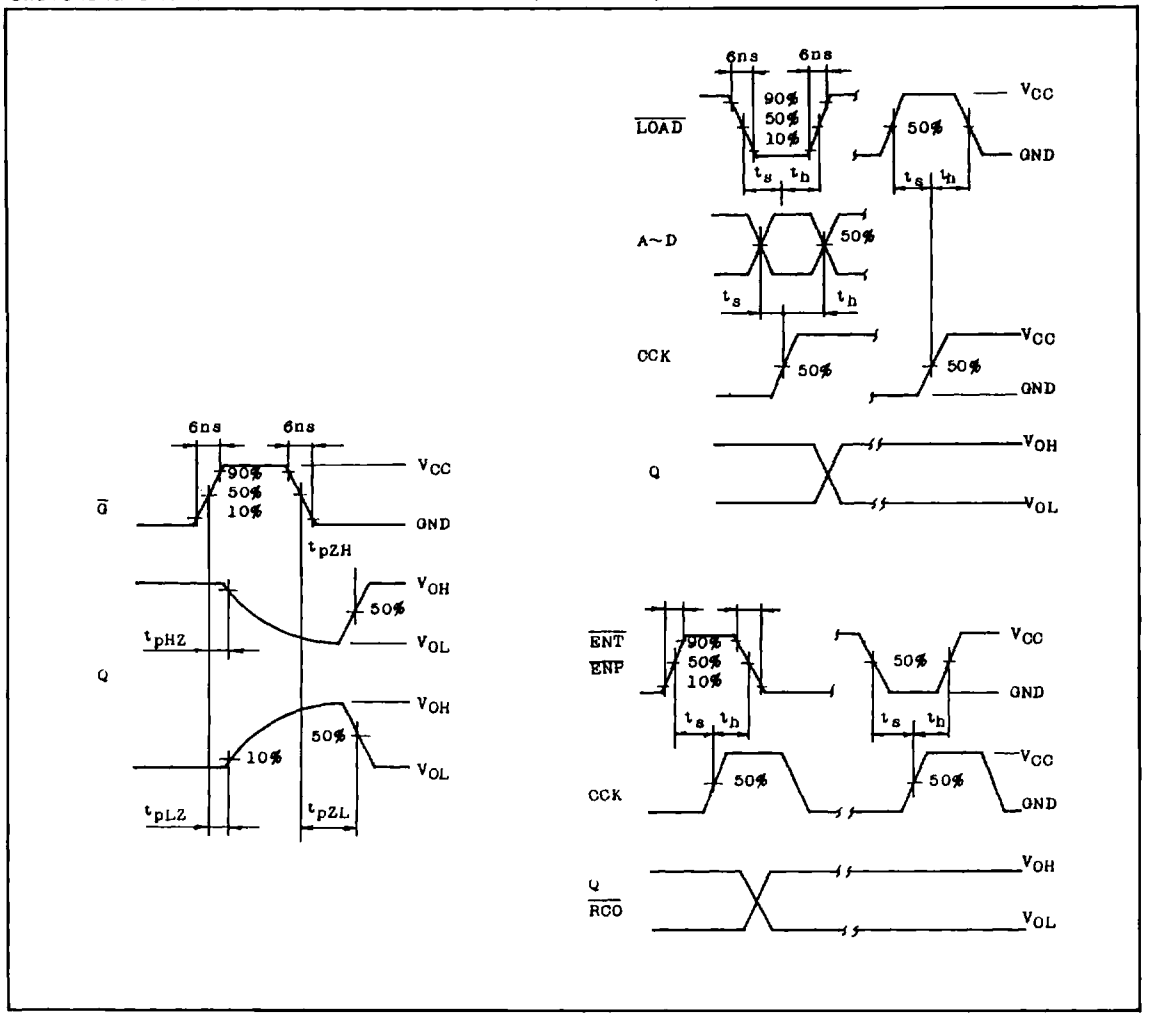








SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



I_{CC}(Opr.) TEST CIRCUIT