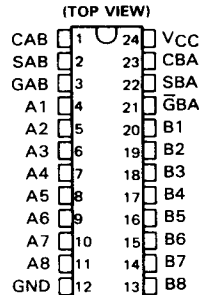


SN54HC651, SN54HC652, SN74HC651, SN74HC652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

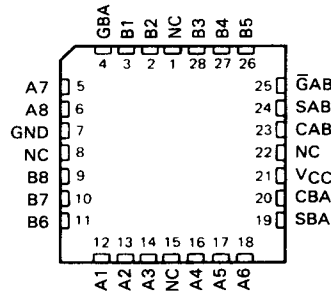
D2684, DECEMBER 1982—REVISED JUNE 1989

- Bus Transceivers and Registers
- Independent Registers and Enables for A and B Buses
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC651, SN54HC652 ... JT PACKAGE
SN74HC651, SN74HC652 ... DW or NT PACKAGE



SN54HC651, SN54HC652 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\bar{G}BA$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The examples on the following page demonstrate the four fundamental bus-management functions that can be performed with the 'HC651 and 'HC652.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\bar{G}BA$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54HC651 and SN54HC652 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC651 and SN74HC652 are characterized for operation from -40°C to 85°C .

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HCMOS Devices

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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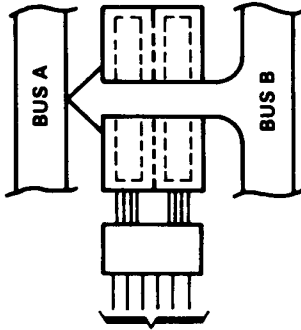
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SN54HC651, SN54HC652, SN74HC651, SN74HC652
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

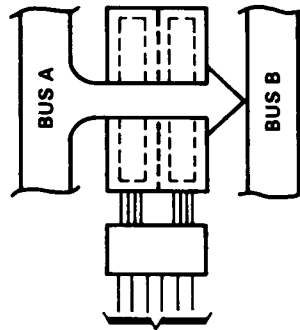
2

HCMOS Devices



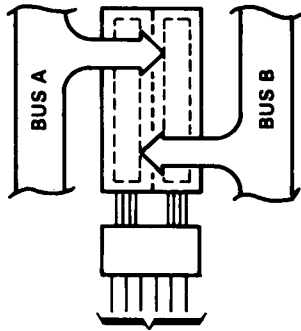
(3)	(21)	(1)	(23)	(2)	(22)
GAB	\bar{G} BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



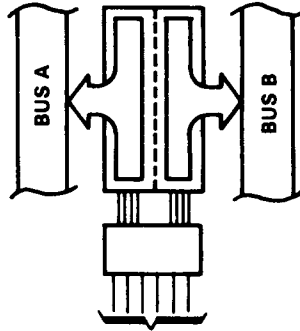
(3)	(21)	(1)	(23)	(2)	(22)
GAB	\bar{G} BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(3)	(21)	(1)	(23)	(2)	(22)
GAB	\bar{G} BA	CAB	CBA	SAB	SBA
X	H	†	X	X	X
L	X	X	†	X	X
L	H	†	†	X	X

STORAGE FROM
A AND/OR B



(3)	(21)	(1)	(23)	(2)	(22)
GAB	\bar{G} BA	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

Pin numbers shown are for DW, JT, and NT packages.

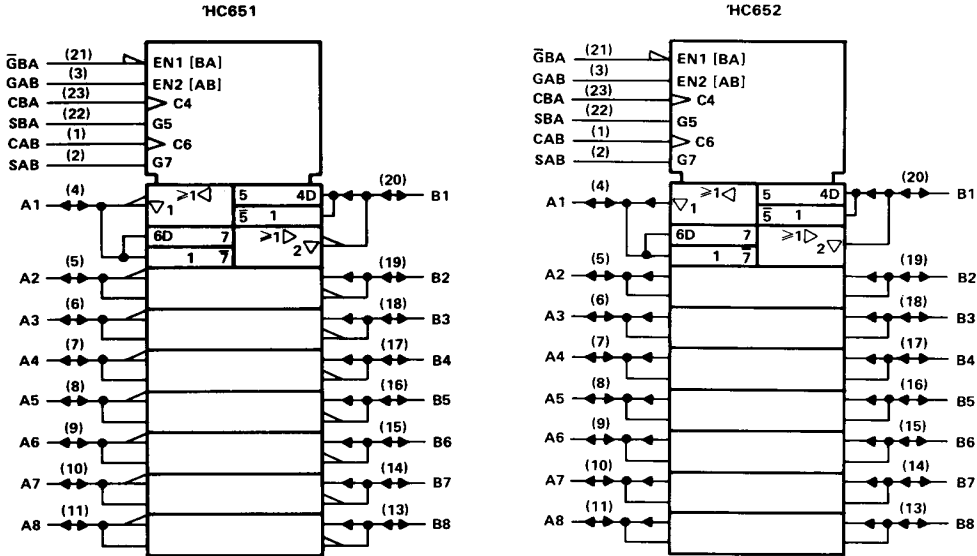
SN54HC651, SN54HC652, SN74HC651, SN74HC652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
GAB	G̅BA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	HC651	HC652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	†	†	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	†	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	†	†	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	†	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	†	†	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B̅ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B̅ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A̅ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored A̅ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A̅ Data to B Bus and Stored B̅ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

†The data output functions may be enabled or disabled by various signals at the GAB and G̅BA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols‡



‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

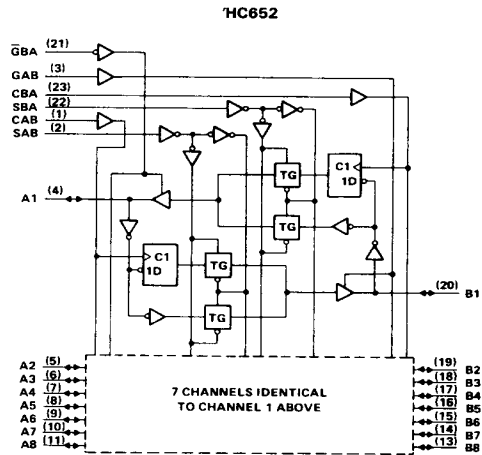
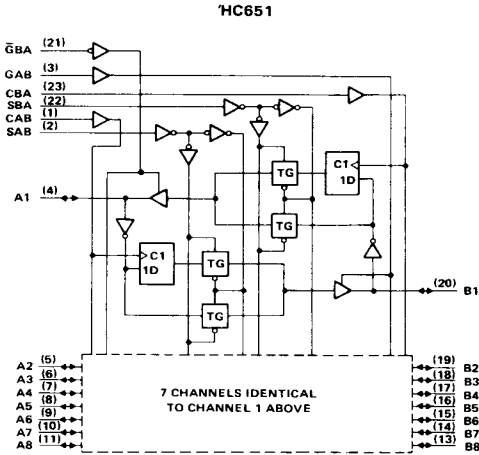
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SN54HC651, SN54HC652, SN74HC651, SN74HC652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

logic diagrams (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300 °C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260 °C
Storage temperature range	-65 °C to 150 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2
HCMOS Devices

**SN54HC651, SN54HC652, SN74HC651, SN74HC652
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS**

recommended operating conditions

		SN54HC651 SN54HC652			SN74HC651 SN74HC652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6\text{ V}$		1.5 3.15 4.2	1.5 3.15 4.2			V
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6\text{ V}$		0 0 0	0.3 0.9 1.2	0 0 0	0.3 0.9 1.2	V
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) times	$V_{CC} = 2\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6\text{ V}$		0 0 0	1000 500 400	0 0 0	1000 500 400	ns
T_A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC651 SN54HC652		SN74HC651 SN74HC652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20\ \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -7.8\text{ mA}$	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20\ \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	4.5 V		0.17	0.26		0.4		0.33		
	6 V		0.15	0.26		0.4		0.33		
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 7.8\text{ mA}$	6 V				0.4		0.33		
I_I	Control Inputs	$V_I = V_{CC}$ or 0	6 V	± 0.1	± 100		± 1000		± 1000	nA
I_{OZ}	A or B	$V_O = V_{CC}$ or GND	6 V	± 0.01	± 0.5		± 10		± 5	μA
I_{CC}		$V_I = V_{CC}$ or 0, $I_O = 0$	6 V		8		160		80	μA
C_I	Control Inputs		2 to 6 V	3	10		10		10	pF

2

HCMOS Devices



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**SN54HC651, SN54HC652, SN74HC651, SN74HC652
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS**

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HC651 SN54HC652		SN74HC651 SN74HC652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
		f _{clock} Clock frequency	2 V 4.5 V 6 V	0 0 0	6 31 36	0 0 0	4.3 22 25	
t _w Pulse duration, CBA or CAB high or low	2 V 4.5 V 6 V	80 16 14		115 23 20		95 19 16		ns
t _{su} Setup time, A before CAB† or B before CBA†	2 V 4.5 V 6 V	100 20 17		150 30 26		125 25 21		ns
t _h Hold time, A after CAB† or B after CBA†	2 V 4.5 V 6V	5 5 5		5 5 5		5 5 5		ns

2

HCMS Devices

**SN54HC651, SN54HC652, SN74HC651, SN74HC652
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS**

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50$ pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25 °C			SN54HC651 SN54HC652		SN74HC651 SN74HC652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	6	10		4.3		5.5	MHz	
			4.5 V	31	40		22		27		
			6 V	36	45		25		31		
t _{pd}	CBA or CAB	A or B	2 V		65	180		270		225	ns
			4.5 V		18	36		54		45	
			6 V		14	31		46		38	
t _{pd}	A or B	B or A	2 V		50	135		205		170	ns
			4.5 V		14	27		41		34	
			6 V		11	23		35		29	
t _{pd}	SBA or SAB†	A or B	2 V		70	190		285		240	ns
			4.5 V		20	38		57		48	
			6 V		16	32		48		41	
t _{en}	$\overline{\text{GBA}}$ or GAB	A or B	2 V		85	245		370		305	ns
			4.5 V		25	49		74		61	
			6 V		20	42		63		52	
t _{dis}	$\overline{\text{GBA}}$ or GAB	A or B	2 V		50	245		370		305	ns
			4.5 V		23	49		74		61	
			6 V		20	42		63		52	
t _t		Any	2 V		28	60		90		75	ns
	4.5 V			8	12		18		15		
	6 V			6	10		15		13		

2

HCMOS Devices

C _{pd}	Power dissipation capacitance	No load, T _A = 25 °C	50 pF typ
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 150$ pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25 °C			SN54HC651 SN54HC652		SN74HC651 SN74HC652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	CBA or CAB	A or B	2 V		90	265		400		330	ns
			4.5 V		24	53		80		66	
			6 V		18	46		68		57	
t _{pd}	A or B	B or A	2 V		70	220		335		275	ns
			4.5 V		20	44		70		55	
			6 V		15	38		57		48	
t _{pd}	SBA or SAB†	A or B	2 V		80	275		415		345	ns
			4.5 V		24	55		83		69	
			6 V		20	47		70		60	
t _{en}	$\overline{\text{GBA}}$ or GAB	A or B	2 V		100	330		500		410	ns
			4.5 V		33	66		100		82	
			6 V		27	57		85		71	
t _t		Any	2 V		45	210		315		265	ns
	4.5 V			17	42		63		53		
	6 V			13	36		53		43		

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.



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