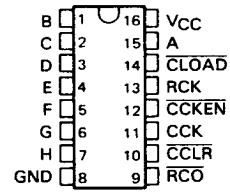
TYPES SN54HC592, SN54HC593, SN74HC592, SN74HC593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

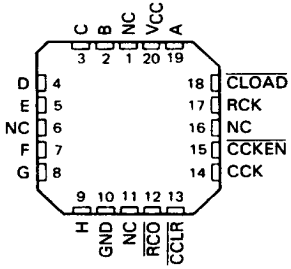
D2684, DECEMBER 1982—REVISED MARCH 1984

- **Parallel Register Inputs ('HC592)**
- **Parallel 3-State I/O: Register Inputs/ Counter Outputs ('HC593)**
- **Counter Has Direct Overriding Load and Clear**
- **High-Current Outputs Can Drive up to 15 LSTTL Loads ('HC593)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC592 . . . J PACKAGE
SN74HC592 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC592 . . . FH OR FK PACKAGE
SN74HC592 . . . FH OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

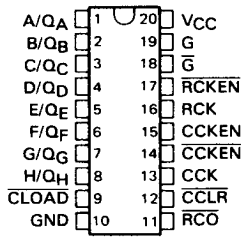
description

The 'HC592 consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive-edge-triggered clocks. In addition, the counter has direct load and clear functions. Expansion is easily accomplished by connecting $\overline{RCO}$ of the first stage to the count enable of the second stage, etc.

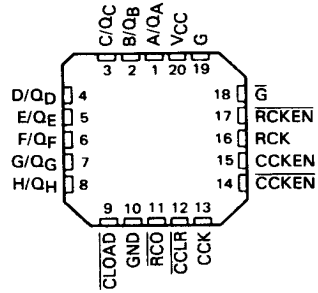
The 'HC593 has all the features of the 'HC592 plus 3-state I/O, which provides parallel counter outputs.

The SN54HC592 and SN54HC593 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC592 and SN74HC593 are characterized for operation from −40°C to 85°C.

SN54HC593 . . . J PACKAGE
SN74HC593 . . . J OR N PACKAGE
(TOP VIEW)



SN54HC593 . . . FH OR FK PACKAGE
SN74HC593 . . . FH OR FN PACKAGE
(TOP VIEW)



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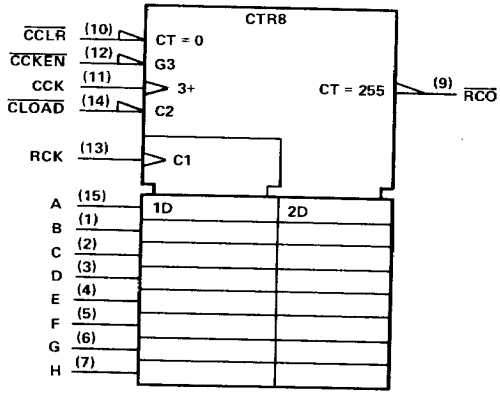
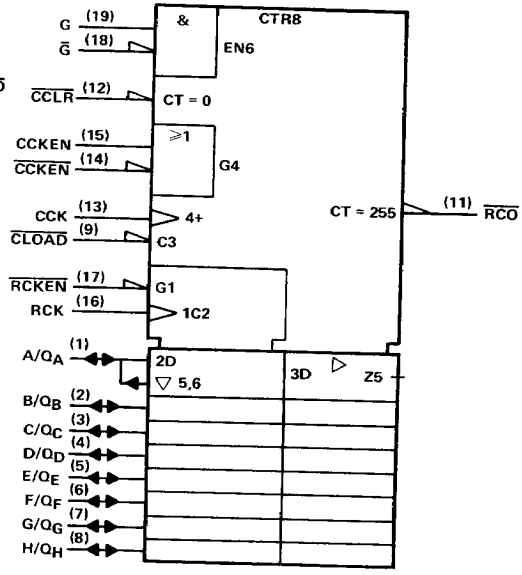
logic symbols

'HC592



'HC593



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

'HC592: See Table IV, page 2-10.
'HC593: See Table III, page 2-8.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC'		SN74HC'		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock} Clock frequency, CCK or RCK		2 V	0	3.3					MHz
		4.5 V	0	17					
		6 V	0	19					
t_w Pulse duration	CCK or RCK high or low	2 V	150						ns
		4.5 V	30						
		6 V	26						
	$\overline{CCLR}$ low	2 V	125						ns
		4.5 V	25						
		6 V	21						
	$\overline{CLOAD}$ low	2 V	125						ns
		4.5 V	25						
		6 V	21						
t_{su} Setup time	$\overline{CCKEN}$ low before CCK	2 V	125						ns
		4.5 V	25						
		6 V	21						
	$\overline{CCLR}$ high (inactive) before CLK↑	2 V	125						ns
		4.5 V	25						
		6 V	21						
	RCK↑ before CCK↑ (see Note 1)	2 V	200						ns
		4.5 V	40						
		6 V	34						
	Data A thru H before RCK↑	2 V	125						ns
		4.5 V	25						
		6 V	21						
t_h Hold time		2 V	5						ns
		4.5 V	5						
		6 V	5						

NOTE 1: The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register outputs.

'HC592 switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC592		SN74HC592		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CCK or RCK		2 V	3.3	8						MHz
			4.5 V	17	35						
			6 V	19	40						
t_{pd}	CCK↑	$\overline{RCO}$	2 V		75						ns
			4.5 V		25						
			6 V		21						
t_{pd}	$\overline{CLOAD}$↓	$\overline{RCO}$	2 V		75						ns
			4.5 V		25						
			6 V		21						
t_{PHL}	$\overline{CCLR}$↓	$\overline{RCO}$	2 V		85						ns
			4.5 V		28						
			6 V		24						
t_{pd}	RCK↑	$\overline{RCO}$	2 V		105						ns
			4.5 V		35						
			6 V		30						

NOTE 2: For load circuits and voltage waveforms, see page 1-14.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC593		SN74HC593		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CCK or RCK		2 V	3.3	8						MHz
			4.5 V	17	35						
			6 V	19	40						
t_{pd}	CCK ↑	Q	2 V		75						ns
			4.5 V		25						
			6 V		21						
t_{pd}	CCK ↑	$\overline{RCO}$	2 V		75						ns
			4.5 V		25						
			6 V		21						
t_{pd}	$\overline{CLOAD}$ ↓	Q	2 V		75						ns
			4.5 V		25						
			6 V		21						
t_{pd}	$\overline{CLOAD}$ ↓	$\overline{RCO}$	2 V		75						ns
			4.5 V		25						
			6 V		21						
t_{pd}	RCK ↑	$\overline{RCO}$	2 V		105						ns
			4.5 V		35						
			6 V		30						
t_{PHL}	$\overline{CCLR}$ ↓	Q	2 V		90						ns
			4.5 V		30						
			6 V		26						
t_{PHL}	$\overline{CCLR}$ ↓	$\overline{RCO}$	2 V		90						ns
			4.5 V		30						
			6 V		26						
t_{en}	G ↑	Q	2 V		66						ns
			4.5 V		22						
			6 V		19						
t_{en}	$\overline{G}$ ↓	Q	2 V		75						ns
			4.5 V		25						
			6 V		21						
t_{dis}	G ↓	Q	2 V		60						ns
			4.5 V		20						
			6 V		17						
t_{dis}	$\overline{G}$ ↑	Q	2 V		60						ns
			4.5 V		20						
			6 V		17						
t_t			2 V		28						ns
			4.5 V		8						
			6 V		6						

NOTE 1: For load circuit and voltage waveforms, see page 1-14.