

## MM54HC4060/MM74HC4060 14 Stage Binary Counter

### General Description

The MM54HC4060/MM74HC4060 is a high speed binary ripple carry counter. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4060 is a 14-stage counter, which device increments on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input. The 'HC4060 also has two additional inputs to enable easy connection of either an RC or crystal oscillator.

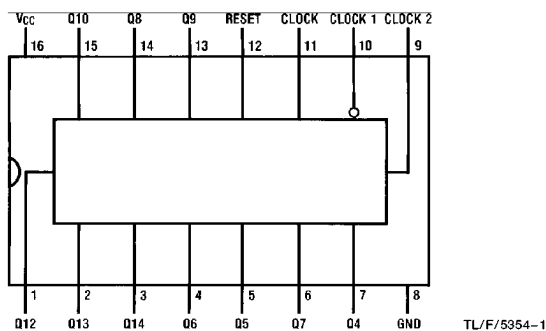
This device is pin equivalent to the CD4060. All inputs are protected from damage due to static discharge by protection diodes to  $V_{CC}$  and ground.

### Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1  $\mu$ A maximum
- Low quiescent current: 80  $\mu$ A maximum (74 Series)
- Output drive capability: 10 LS-TTL loads

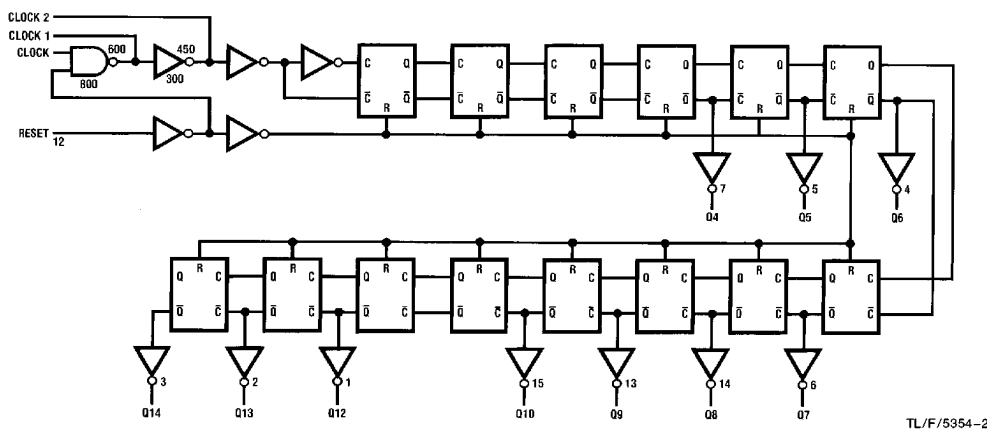
### Connection and Logic Diagrams

Dual-In-Line Package



Top View

Order Number MM54HC4060 or MM74HC4060



## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IH}$ )	-1.5 to $V_{CC}$ + 1.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC}$ + 0.5V
Clamp Diode Current ( $I_{CD}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

## DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		74HC	54HC	Units					
				$T_A = -40$ to $85^\circ C$ $T_A = -55$ to $125^\circ C$									
				Typ					Guaranteed Limits				
$V_{IH}$	Minimum High Level Voltage (Not Applicable to Pins 9 & 10)		2.0V		1.5	1.5	1.5	V					
			4.5V		3.15	3.15	3.15	V					
			6.0V		4.2	4.2	4.2	V					
$V_{IL}$	Maximum Low Level Input Voltage ** (Not Applicable to Pins 9 & 10)		2.0V		0.5	0.5	0.5	V					
			4.5V		1.35	1.35	1.35	V					
			6.0V		1.8	1.8	1.8	V					
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V					
			4.5V	4.5	4.4	4.4	4.4	V					
			6.0V	6.0	5.9	5.9	5.9	V					
		Except Pins 9 & 10	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V				
				6.0V	5.7	5.48	5.34	5.2	V				
		Pins 9 & 10	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 0.4$ mA $ I_{OUT}  = 0.52$ mA			3.98	3.84	3.7	V				
				5.48	5.34	5.2	V						
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V					
			4.5V	0	0.1	0.1	0.1	V					
			6.0V	0	0.1	0.1	0.1	V					
		Except Pins 9 & 10	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V				
				6.0V	0.2	0.26	0.33	0.4	V				
		Pins 9 & 10	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  = 0.4$ mA $ I_{OUT}  = 0.52$ mA			0.26	0.33	0.4	V				
				0.26	0.33	0.4	V						
$I_{IH}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$					
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	$\mu A$					

**Note 1:** Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating: plastic "N" package: -12 mW/°C from 65°C to 85°C ceramic "J" package: -12 mW/°C from 100°C to 125°C

**Note 4:** For a power supply of 5V  $\pm 10\%$  the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\*  $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

## AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Clock Frequency			30	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay to $Q_4$	(Note 5)	40	20	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay to any Q		16	40	ns
$t_{REM}$	Minimum Reset Removal Time		10	20	ns
$t_W$	Minimum Pulse Width		10	16	ns

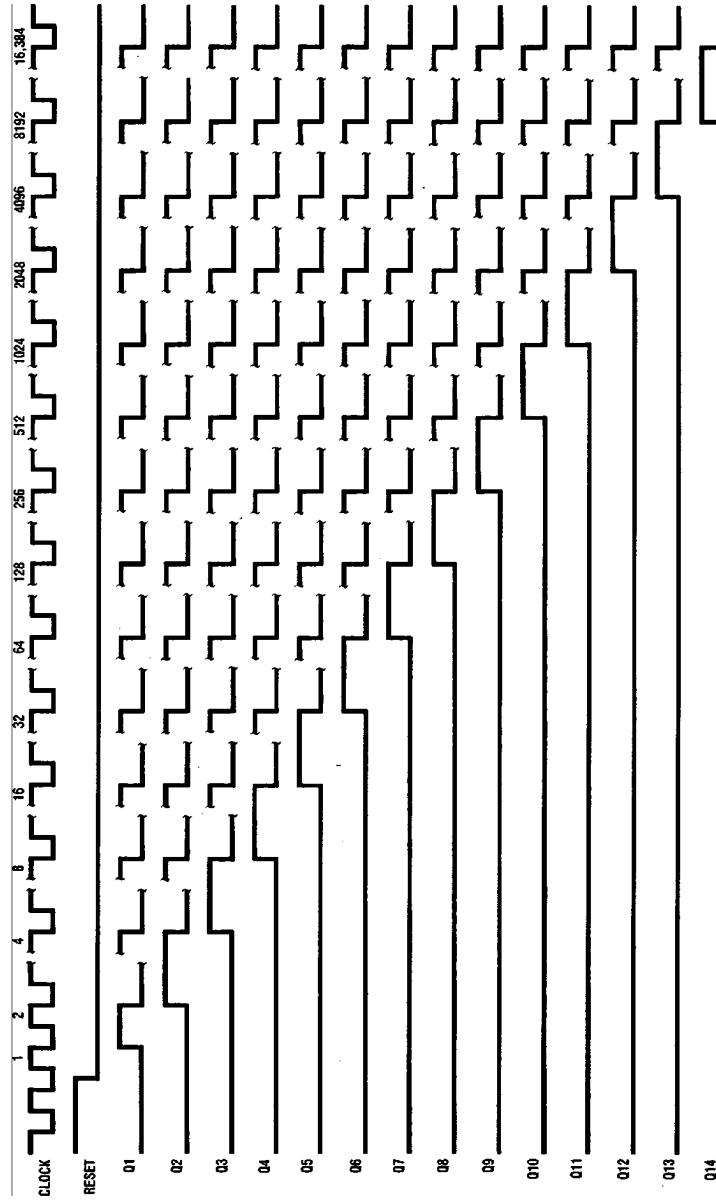
## AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$ , $C_L = 50\text{ pF}$ , $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A 74HC$	$T_A 54HC$	Units	
				Typ	Guaranteed Limits				
						$T_A = -40\text{ to }85^\circ C$	$T_A = -55\text{ to }125^\circ C$		
$f_{MAX}$	Maximum Operating Frequency		2.0V		6	5	4	MHz	
			4.5V		30	24	20	MHz	
			6.0V		35	28	24	MHz	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay Clock to $Q_4$		2.0V	120	380	475	171	ns	
			4.5V	42	76	95	114	ns	
			6.0V	35	65	81	97	ns	
$t_{PHL}$	Maximum Propagation Delay Reset to any Q		2.0V	72	240	302	358	ns	
			4.5V	24	48	60	72	ns	
			6.0V	20	41	51	61	ns	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay Between Stages $Q_n$ to $Q_{n+1}$		2.0V		125	156	188	ns	
			4.5V		25	31	38	ns	
			6.0V		21	26	31	ns	
$t_{REM}$	Minimum Reset Removal Time		2.0V		100	125	150	ns	
			4.5V		20	25	30	ns	
			6.0V		17	21	25	ns	
$t_W$	Minimum Pulse Width		2.0V		80	100	120	ns	
			4.5V		16	20	24	ns	
			6.0V		14	17	20	ns	
$t_r$ , $t_f$	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns	
			4.5V		500	500	500	ns	
			6.0V		400	400	400	ns	
$t_{THL}$ , $t_{TLH}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns	
			4.5V	10	15	19	22	ns	
			6.0V	9	13	16	19	ns	
$C_{PD}$	Power Dissipation Capacitance (Note 6)	(per package)		55				pF	
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF	

**Note 5:** Typical Propagation delay time to any output can be calculated using:  $t_p = 17 + 12(N-1)\text{ ns}$ ; where N is the number of the output,  $Q_W$ , at  $V_{CC} = 5V$ .

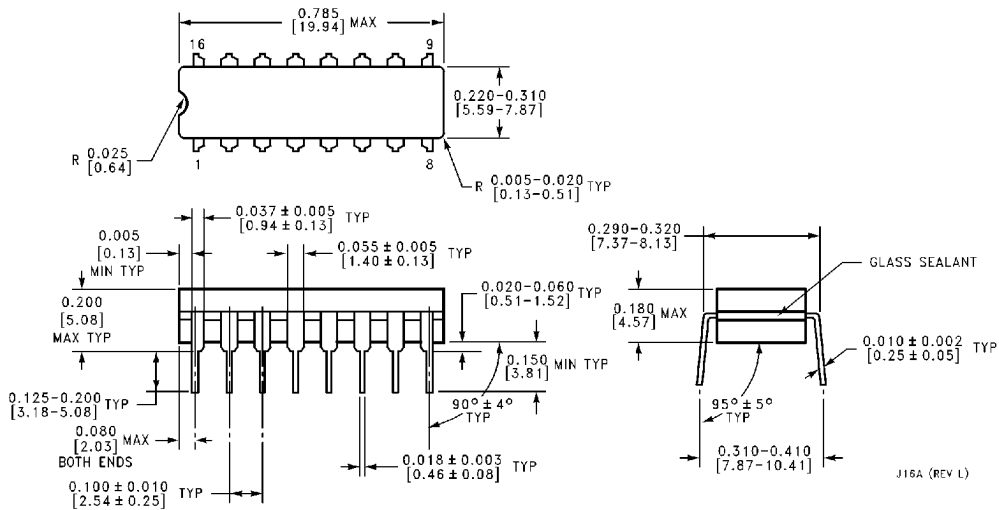
**Note 6:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

# Timing Diagram



TL/F/5954-3

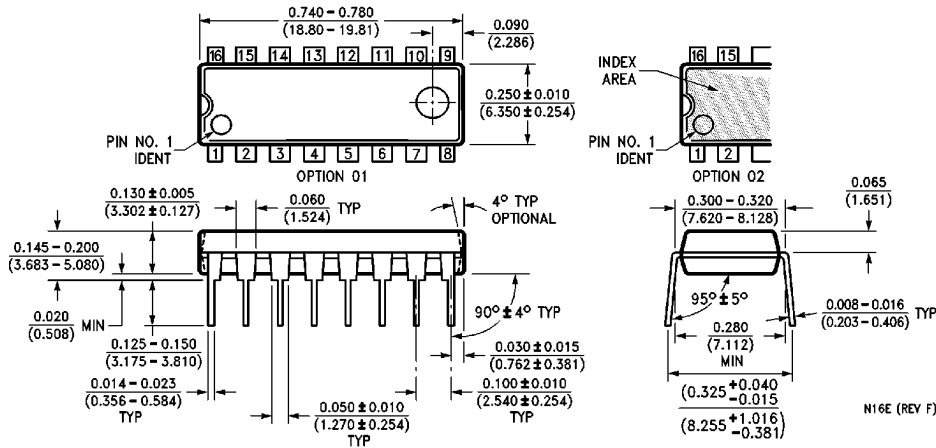
**Physical Dimensions** inches (millimeters)



**Order Number MM54HC4060J**  
**NS Package J16A**

J16A (REV L)

Physical Dimensions inches (millimeters) (Continued)



Order Number MM74HC4060J, N  
NS Package N16E

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