8-BIT SYNCHRONOUS BINARY DOWN COUNTER

FEATURES

- **Cascadable**
- **Synchronous or asynchronous preset**
- **Output capability: standard**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT40103 are high-speed Si-gate CMOS devices and are pin compatible with the "40103" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40103 consist each of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The "40103" contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ($\overline{TC}$) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P_0 to P_7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$.
When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P_0 to P_7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P_0 to P_7) represent a single 8-bit binary word.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	C_L = 15 pF; V_{CC} = 5 V	30	30	ns
f_{max}	maximum clock frequency		32	31	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	27	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP	clock input (LOW-to-HIGH, edge-triggered)
2	$\overline{MR}$	asynchronous master reset input (active LOW)
3	$\overline{TE}$	terminal enable input
4, 5, 6, 7, 10, 11, 12, 13	P_0 to P_7	jam inputs
8	GND	ground (0 V)
9	$\overline{PL}$	asynchronous preset enable input (active LOW)
14	$\overline{TC}$	terminal count output (active LOW)
15	$\overline{PE}$	synchronous preset enable input (active LOW)
16	V_{CC}	positive supply voltage

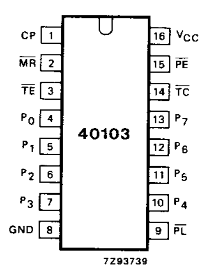

Fig. 1 Pin configuration.

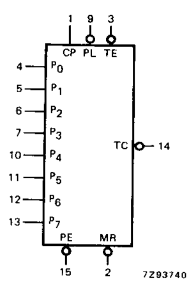

Fig. 2 Logic symbol.

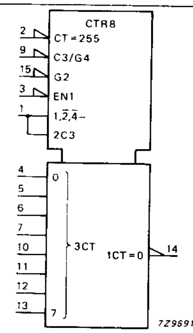

Fig. 3 IEC logic symbol.

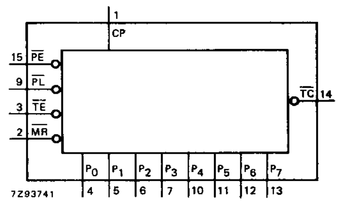

Fig. 4 Functional diagram.

FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	synchronous	inhibit counter
H	H	H	L		count down
H	H	L	X		preset on next LOW-to HIGH clock transition
H	L	X	X	asynchronous	preset asynchronously
L	X	X	X		clear to maximum count

Notes to function table

1. Clock connected to CP.
2. Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
3. Jam inputs: MSD = P_7, LSD = P_0.

H = HIGH voltage level
L = LOW voltage level
X = don't care

GENERAL DESCRIPTION (Cont'd)

When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the function table.

If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.
The "40103" may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output, in either a synchronous or ripple mode.

APPLICATIONS

- **Divide-by-n counters**
- **Programmable timers**
- **Interrupt timers**
- **Cycle/program counters**

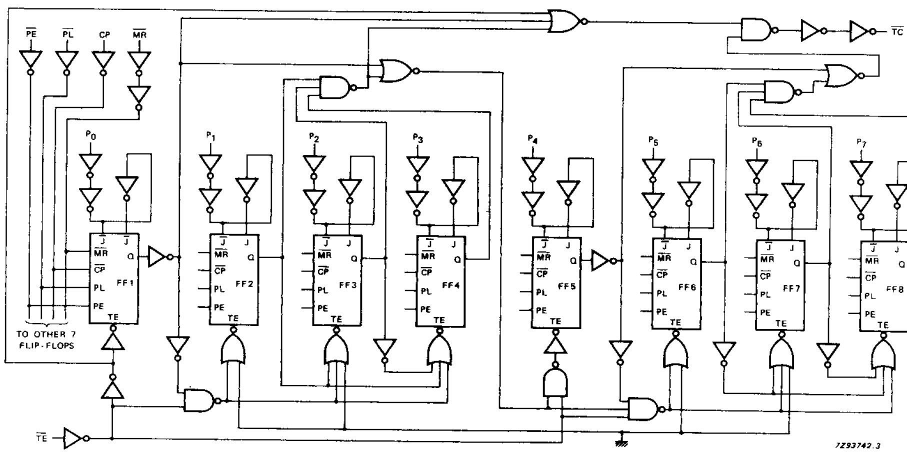

Fig. 5 Logic diagram.

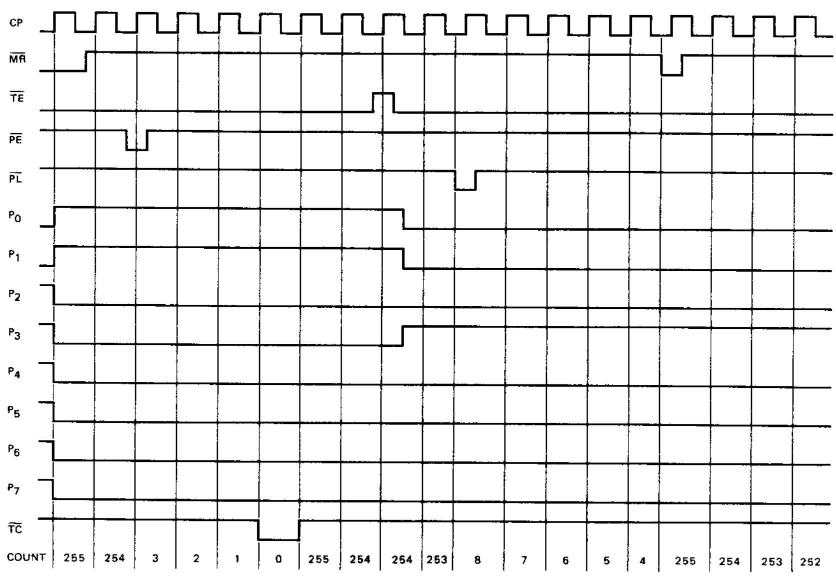

Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	TEST CONDITIONS V_{CC} V	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$		96 35 28	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}/t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}$		102 37 30	315 63 53		395 79 40		475 95 81	ns	2.0 4.5 6.0	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$		83 30 24	275 55 47		345 69 59		415 83 71	ns	2.0 4.5 6.0	Fig. 9
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 7 and 8
t_W	clock pulse width HIGH or LOW	165 33 28	22 8 6		205 41 35		250 50 43		ns	2.0 4.5 6.0	Fig. 7
t_W	master reset pulse width LOW	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t_W	preset enable pulse width $\overline{PL}$; LOW	125 25 21	33 12 10		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP or $\overline{PL}$ to CP	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $\overline{TE}$ to CP	150 30 26	44 16 13		190 38 33		225 45 38		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time P_n to CP	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig. 12
t_h	hold time $\overline{PE}$ to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11

AC CHARACTERISTICS FOR 74HC (Cont'd)

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time $\overline{TE}$ to CP	0 0 0	−30 −11 −9		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 11
t_h	hold time P_n to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 12
f_{max}	maximum clock pulse frequency	3.0 15 18	10 29 35		2.4 12 14		2.0 10 12		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
CP, $\overline{PE}$	1.50
$\overline{MR}$	1.00
$\overline{TE}$	0.80
$\overline{PL}$	0.35
P_n	0.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to $\overline{TC}$		35	60		75		90	ns	4.5	Fig. 7
t_{PHL}/ t_{PLH}	propagation delay $\overline{TE}$ to $\overline{TC}$		23	40		50		60	ns	4.5	Fig. 8
t_{PHL}/ t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}$		44	75		94		112	ns	4.5	Fig. 9
t_{PHL}	propagation delay $\overline{MR}$ to $\overline{TC}$		29	55		69		83	ns	4.5	Fig. 9
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs. 7 and 8
t_W	clock pulse width HIGH or LOW	33	10		41		50		ns	4.5	Fig. 7
t_W	master reset pulse width LOW	30	16		38		45		ns	4.5	Fig. 9
t_W	preset enable pulse width $\overline{PL}$; LOW	38	22		48		57		ns	4.5	Fig. 9
t_{rem}	removal time $\overline{MR}$ to CP or $\overline{PL}$ to CP	10	1		13		15		ns	4.5	Fig. 10
t_{su}	set-up time $\overline{PE}$ to CP	20	11		25		30		ns	4.5	Fig. 11
t_{su}	set-up time $\overline{TE}$ to CP	40	20		50		60		ns	4.5	Fig. 11
t_{su}	set-up time P_n to CP	20	11		25		30		ns	4.5	Fig. 12
t_h	hold time $\overline{PE}$ to CP	2	−3		2		2		ns	4.5	Fig. 11

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_h	hold time $\overline{TE}$ to CP	0	−10		0		0		ns	4.5	Fig. 11
t_h	hold time P_n to CP	0	−5		0		0		ns	4.5	Fig. 12
f_{max}	maximum clock pulse frequency	15	28		12		10		MHz	4.5	Fig. 7

AC WAVEFORMS

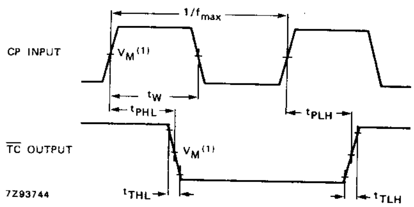

Fig. 7 Waveforms showing the clock input (CP) to $\overline{TC}$ propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

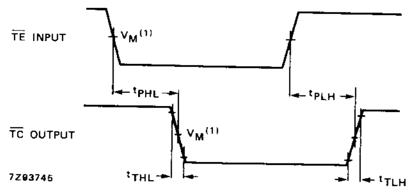

Fig. 8 Waveforms showing the $\overline{TE}$ to $\overline{TC}$ propagation delays.

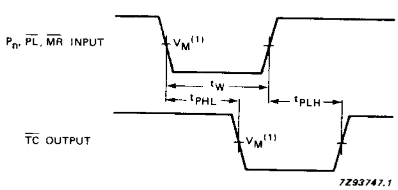

Fig. 9 Waveforms showing $\overline{PL}$, $\overline{MR}$, P_n to $\overline{TC}$ propagation delays.

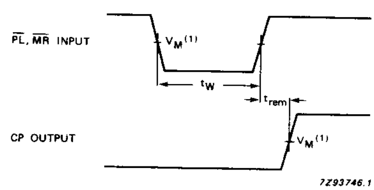

Fig. 10 Waveforms showing removal time for $\overline{MR}$ and $\overline{PL}$.

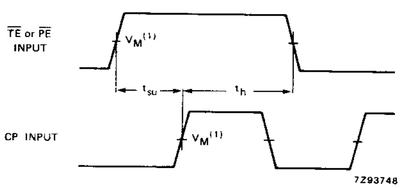

Fig. 11 Waveforms showing hold and set-up times for $\overline{MR}$ or $\overline{PE}$ to CP.

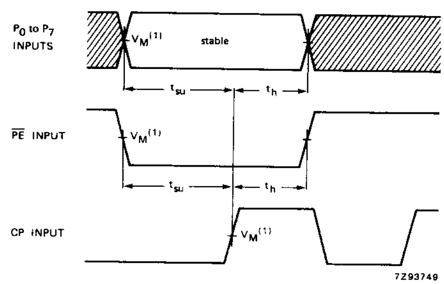

Fig. 12 Waveforms showing hold and set-up times for P_n, $\overline{PE}$ to CP.

Note to AC waveforms

(1) HC : $V_M = 50\%$; V_I = GND to V_{CC}.
HCT: $V_M = 1.3$ V; V_I = GND to 3 V.

Note to Fig. 12

The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION INFORMATION

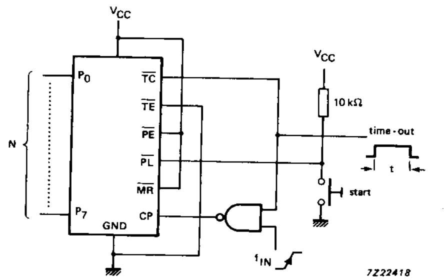

Fig. 13 Programmable timer.

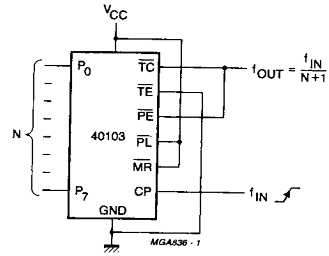

Fig. 14 Divide-by-N counter.