

## HEX BUFFER/LINE DRIVER; 3-STATE

## FEATURES

- Non-inverting outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT367 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT367 are hex non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs (1 $\bar{O}E$ , 2 $\bar{O}E$ ).

A HIGH on n $\bar{O}E$  causes the outputs to assume a high impedance OFF-state. The "367" is identical to the "368" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	8	11	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

## Notes

1. CPD is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz      C<sub>L</sub> = output load capacitance in pF  
f<sub>o</sub> = output frequency in MHz      V<sub>CC</sub> = supply voltage in V  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

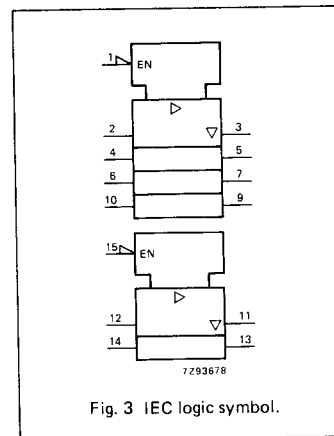
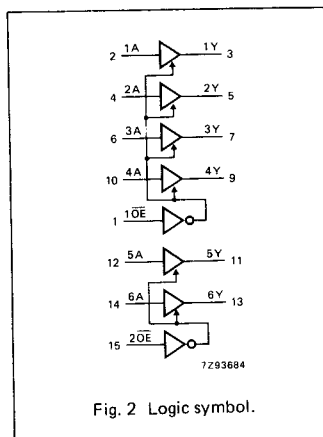
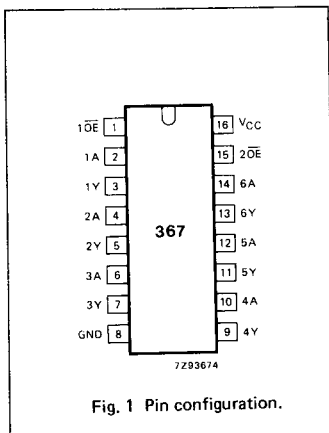
## PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1 $\bar{O}E$ , 2 $\bar{O}E$	output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	data outputs
8	GND	ground (0 V)
16	V <sub>CC</sub>	positive supply voltage



**74HC/HCT367**  
**MSI**

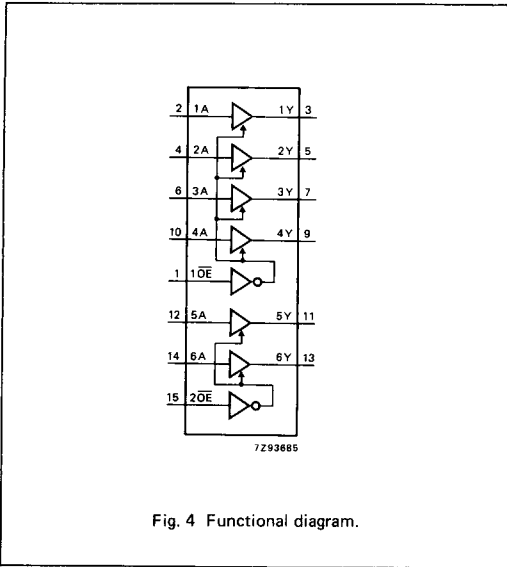


Fig. 4 Functional diagram.

**FUNCTION TABLE**

INPUTS		OUTPUTS
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

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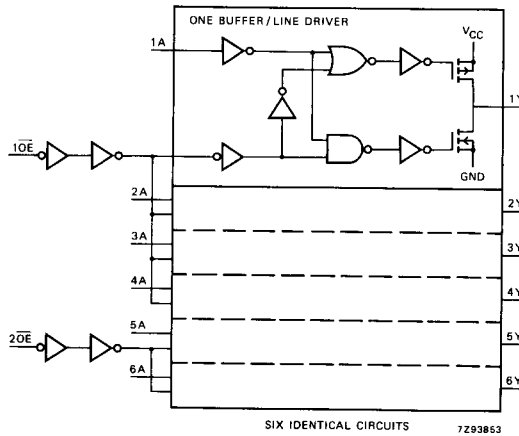


Fig. 5 Logic diagram.

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## Hex buffer/line driver; 3-state

74HC/HCT367

MSI

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS	
		74HC							V <sub>CC</sub> V	WAVEFORMS
		+25		-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig. 6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY	44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY	55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t <sub>THL</sub> / t <sub>TLLH</sub>	output transition time	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

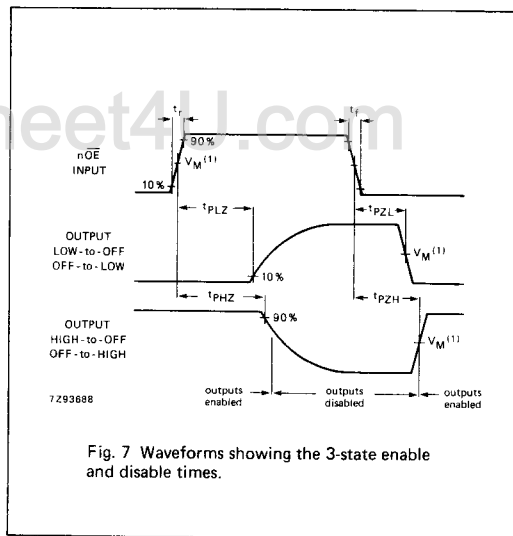
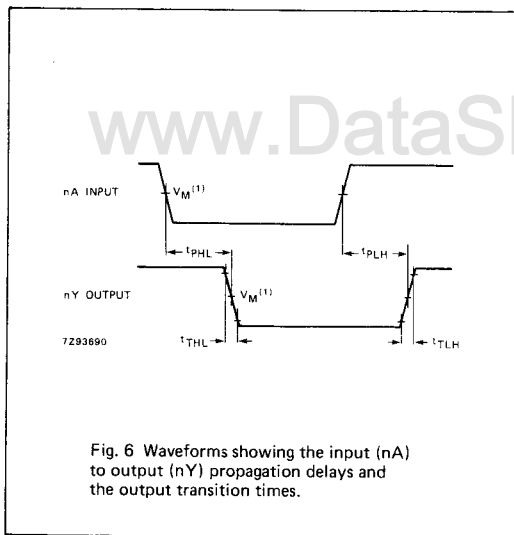
INPUT	UNIT LOAD COEFFICIENT
1OE	1.00
2OE	0.90
nA	1.00

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay nA to nY		14	25		31		38	ns	4.5	Fig. 6
$t_{PZH}/$ $t_{PZL}$	3-state output enable time nOE to nY		16	35		44		53	ns	4.5	Fig. 7
$t_{PHZ}/$ $t_{PLZ}$	3-state output disable time nOE to nY		21	35		44		53	ns	4.5	Fig. 7
$t_{THL}/$ $t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Fig. 6

## AC WAVEFORMS



## Note to AC waveforms

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3$  V;  $V_I = \text{GND to } 3$  V.