National Semiconductor

54F/74F676
16-Bit Serial/Parallel-In, Serial-Out Shift Register

General Description

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data (P_0–P_{15}) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

Features

- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Slim 24 lead 300 mil package

Commercial	Military	Package Number	Package Description
74F676PC		N24A	24-Lead (0.600″ Wide) Molded Dual-In-Line
74F676SPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
	54F676DM (Note 2)	J24A	24-Lead (0.600″ Wide) Ceramic Dual-In-Line
	54F676SDM (Note 2)	J24F	24-Lead (0.300″ Wide) Ceramic Dual-In-Line
74F676SC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
	54F676FM (Note 2)	W24C	24-Lead Cerpack
	54F676LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

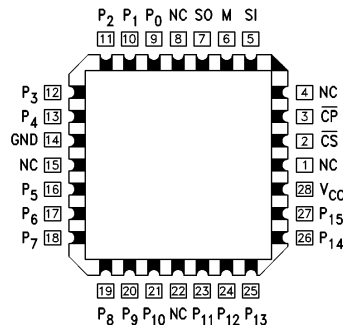**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Connection Diagrams

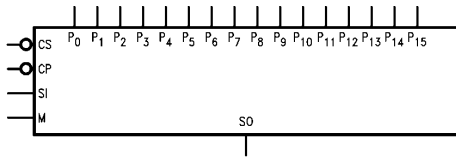**Pin Assignment
for DIP, SOIC and Flatpak**
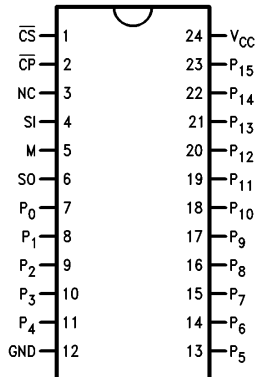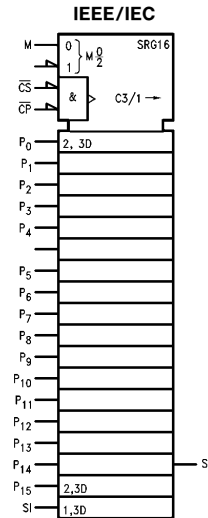

TL/F/9588–2

**Pin Assignment
for LCC**

TL/F/9588–3

Logic Symbols

TL/F/9588–1

IEEE/IEC

TL/F/9588–4

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
P_0–P_{15}	Parallel Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{CP}$	Clock Pulse Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
M	Mode Select Input	1.0/1.0	20 μA/−0.6 mA
SI	Serial Data Input	1.0/1.0	20 μA/−0.6 mA
SO	Serial Output	50/33.3	−1 mA/20 mA

Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD—a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the sixteen registers.

Shift/Serial Load—data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load—data present on P_0–P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

Shift Register Operations Table

Control Input			Operating Mode
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	⌐⌐	Shift/Serial Load
L	H	⌐⌐	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐⌐ = HIGH-to-LOW Transition

Block Diagram

TL/F/9588–5

2
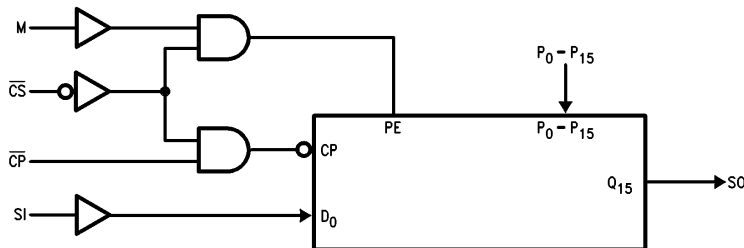
Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$
Plastic	$-55°C$ to $+150°C$

V_{CC} Pin Potential to
Ground Pin $\qquad$ $-0.5V$ to $+7.0V$

Input Voltage (Note 2) $\qquad$ $-0.5V$ to $+7.0V$

Input Current (Note 2) $\qquad$ -30 mA to $+5.0$ mA

Voltage Applied to Output
in HIGH State (with $V_{CC} = 0V$)
Standard Output $\qquad$ $-0.5V$ to V_{CC}
TRI-STATE® Output $\qquad$ $-0.5V$ to $+5.5V$

Current Applied to Output
in LOW State (Max) $\qquad$ twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	$-55°C$ to $+125°C$
Commercial	$0°C$ to $+70°C$
Supply Voltage	
Military	$+4.5V$ to $+5.5V$
Commercial	$+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	$I_{OH} = -1$ mA
		74F 10% V_{CC}	2.5					$I_{OH} = -1$ mA
		74F 5% V_{CC}	2.7					$I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% V_{CC}			0.5			$I_{OL} = 20$ mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	$V_{IN} = 2.7V$
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	$V_{IN} = 7.0V$
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	$V_{OUT} = V_{CC}$
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9$ μA, All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	$V_{IOD} = 150$ mV, All Other Pins Grounded
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I_{CC}	Power Supply Current				72	mA	Max	

AC Electrical Characteristics

Symbol	Parameter	74F T$_A$ = +25°C V$_{CC}$ = +5.0V C$_L$ = 50 pF			54F T$_A$, V$_{CC}$ = Mil C$_L$ = 50 pF		74F T$_A$, V$_{CC}$ = Com C$_L$ = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f$_{max}$	Maximum Clock Frequency	100	110		45		90		MHz
t$_{PLH}$ t$_{PHL}$	Propagation Delay $\overline{CP}$ to SO	4.5 5.0	9.0 9.0	11.0 12.5	4.5 5.0	17.0 14.5	4.5 5.0	12.0 13.5	ns

AC Operating Requirements

Symbol	Parameter	74F T$_A$ = +25°C V$_{CC}$ = +5.0V		54F T$_A$, V$_{CC}$ = Mil		74F T$_A$, V$_{CC}$ = Com		Units
		Min	Max	Min	Max	Min	Max	
t$_s$(H) t$_s$(L)	Setup Time, HIGH or LOW SI to $\overline{CP}$	4.0 4.0		4.0 4.0		4.0 4.0		ns
t$_h$(H) t$_h$(L)	Hold Time, HIGH or LOW SI to $\overline{CP}$	4.0 4.0		4.0 4.0		4.0 4.0		
t$_s$(H) t$_s$(L)	Setup Time, HIGH or LOW P$_n$ to $\overline{CP}$	3.0 3.0		3.0 3.0		3.0 3.0		ns
t$_h$(H) t$_h$(L)	Hold Time, HIGH or LOW P$_n$ to $\overline{CP}$	4.0 4.0		4.0 4.0		4.0 4.0		
t$_s$(H) t$_s$(L)	Setup Time, HIGH or LOW M to $\overline{CP}$	8.0 8.0		8.0 8.0		8.0 8.0		ns
t$_h$(H) t$_h$(L)	Hold Time, HIGH or LOW M to $\overline{CP}$	2.0 2.0		2.0 2.0		2.0 2.0		
t$_s$(L)	Setup Time, LOW $\overline{CS}$ to $\overline{CP}$	10.0		12.0		10.0		ns
t$_h$(H)	Hold Time, HIGH $\overline{CS}$ to $\overline{CP}$	10.0		10.0		10.0		
t$_w$(H) t$_w$(L)	$\overline{CP}$ Pulse Width HIGH or LOW	4.0 6.0		5.0 9.0		4.0 6.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

<u>74F</u>   <u>676</u>   S   C   X

Temperature Range Family
   74F = Commercial
   54F = Military

Device Type

Package Code
   P =   Plastic DIP
   SP =   Slim Plastic DIP
   D =   Ceramic DIP
   SD =   Slim Ceramic DIP
   F =   Flatpak
   L =   Leadless Chip Carrier (LCC)
   S =   Small Outline SOIC JEDEC

Special Variations
   QB = Military grade device with
          environmental and burn-in
          processing

Temperature Range
   C = Commercial (0°C to +70°C)
   M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)

0.015 MIN TYP
PIN #1 INDEX
45° x 0.015±0.010

□0.450 ± 0.008

0.300±0.005 TYP

26   4
0.093
0.077
25   5
R 0.011 TYP
0.007

0.028 TYP
0.022

0.075
0.063

0.003 MIN TYP
0.015 MAX TYP

0.055 TYP
0.045

19
0.055 TYP
0.045

11

0.022 MAX TYP
0.006 MIN TYP

18   12
45° x 0.040±0.010
3 PLCS

0.083 TYP
0.067

DETAIL A   DETAIL A

TOP VIEW

BOTTOM VIEW

SIDE VIEW

E28A (REV D)

28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A

1.290
(32.766)
MAX

0.600
(15.240)
MAX
GLASS

24 23 22 21 20 19 18 17 16 15 14 13

0.025
(0.635)
RAD

0.514−0.526
(13.06−13.36)

1 2 3 4 5 6 7 8 9 10 11 12

0.030−0.055
(0.762−1.397)
RAD TYP

0.590−0.620
(14.986−15.748)

0.005
(0.127)
MIN

GLASS
SEALANT

0.055 ±0.005
(1.397 ±0.127)

0.180
(4.572)
MAX

0.020−0.070
(0.508−1.778)

95° ±5°

0.008−0.012
(0.203−0.305)

0.685 +0.025
−0.060
(17.40 +0.635
−1.524)

0.098
(2.489)
MAX

0.100 ±0.010
(2.540 ±0.254)

0.018 ±0.003
(0.457 ±0.076)

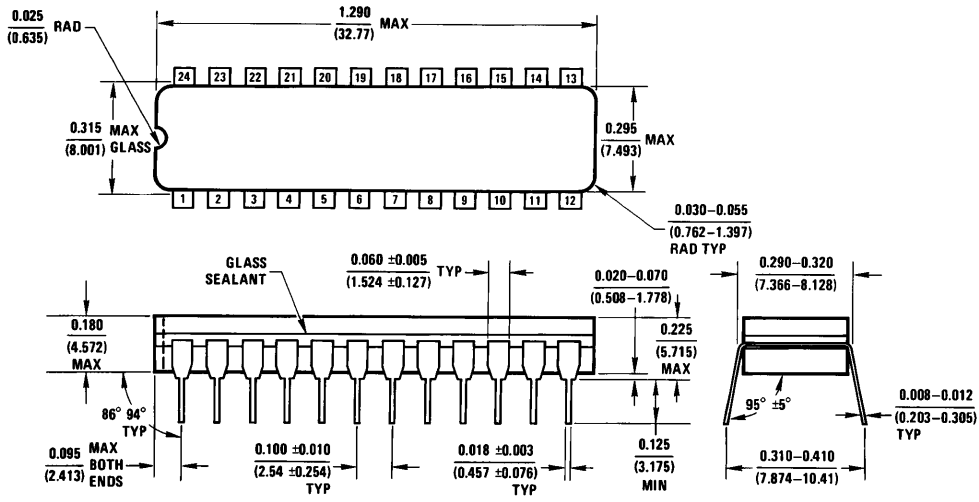86°
94°
TYP

0.125−0.200
(3.175−5.080)
MIN

0.150
(3.810)
MIN

J24A (REV H)
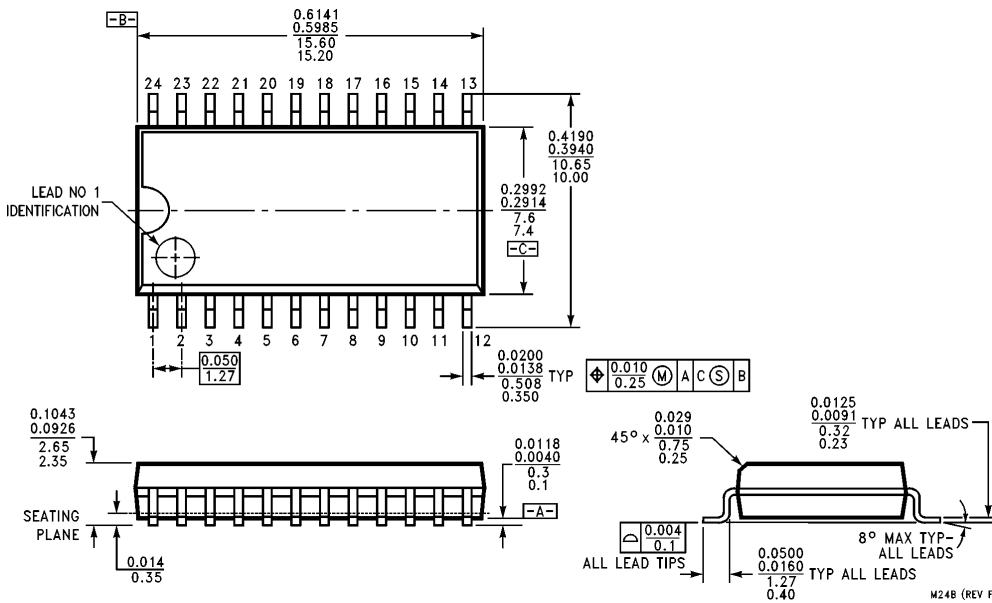
24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24A
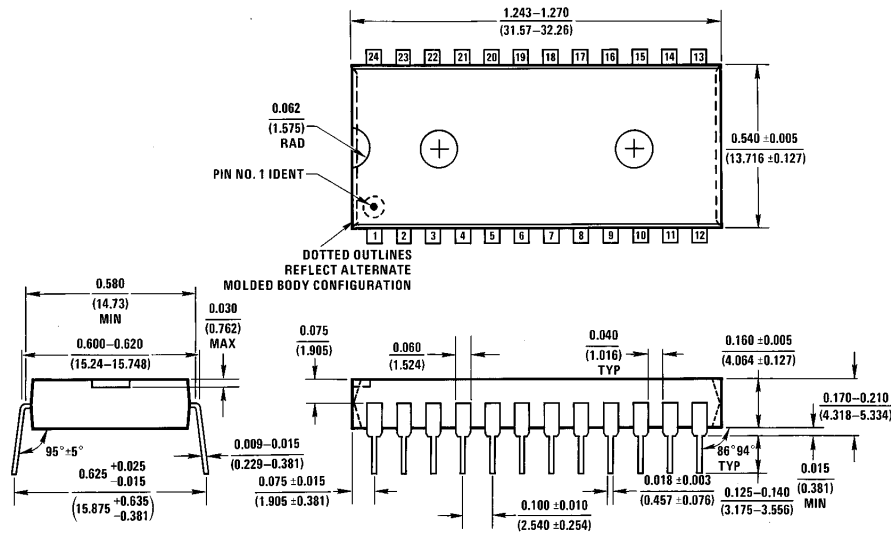
Physical Dimensions inches (millimeters) (Continued)

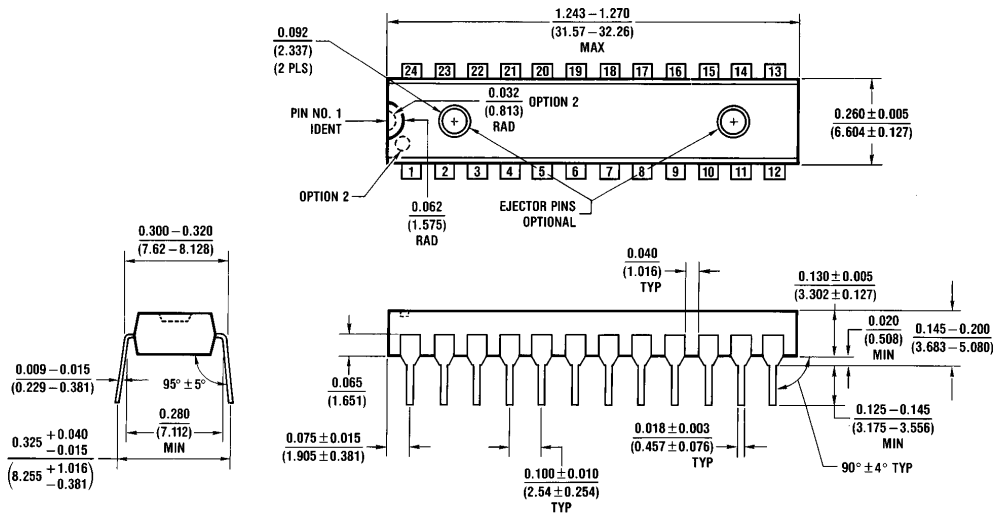24-Lead (0.300″ Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

24-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B

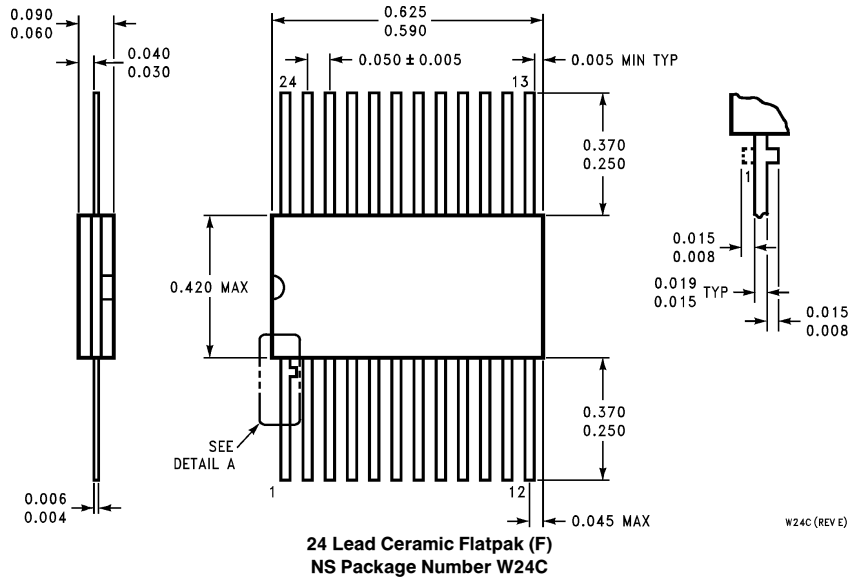# Physical Dimensions inches (millimeters) (Continued)

1.243−1.270
(31.57−32.26)

24 23 22 21 20 19 18 17 16 15 14 13

0.062
(1.575)
RAD

PIN NO. 1 IDENT

0.540 ±0.005
(13.716 ±0.127)

1 2 3 4 5 6 7 8 9 10 11 12

DOTTED OUTLINES
REFLECT ALTERNATE
MOLDED BODY CONFIGURATION

0.580
(14.73)
MIN

0.030
(0.762)
MAX

0.600−0.620
(15.24−15.748)

0.075
(1.905)

0.060
(1.524)

0.040
(1.016)
TYP

0.160 ±0.005
(4.064 ±0.127)

0.170−0.210
(4.318−5.334)

95°±5°

0.009−0.015
(0.229−0.381)

86°94°
TYP

0.015
(0.381)
MIN

0.625 +0.025
−0.015

0.075 ±0.015
(1.905 ±0.381)

0.018 ±0.003
(0.457 ±0.076)

0.125−0.140
(3.175−3.556)

(15.875 +0.635
−0.381)

0.100 ±0.010
(2.540 ±0.254)

N24A (REV E)

24-Lead (0.600″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N24A

1.243 − 1.270
(31.57 − 32.26)
MAX

0.092
(2.337)
(2 PLS)

24 23 22 21 20 19 18 17 16 15 14 13

0.032
(0.813)
RAD

OPTION 2

PIN NO. 1
IDENT

0.260 ± 0.005
(6.604 ± 0.127)

OPTION 2

1 2 3 4 5 6 7 8 9 10 11 12

0.062
(1.575)
RAD

EJECTOR PINS
OPTIONAL

0.300 − 0.320
(7.62 − 8.128)

0.040
(1.016)
TYP

0.130 ± 0.005
(3.302 ± 0.127)

0.020
(0.508)
MIN

0.145 − 0.200
(3.683 − 5.080)

0.009 − 0.015
(0.229 − 0.381)

95° ± 5°

0.065
(1.651)

0.280
(7.112)
MIN

0.125 − 0.145
(3.175 − 3.556)
MIN

0.325 +0.040
−0.015

0.075 ± 0.015
(1.905 ± 0.381)

0.018 ± 0.003
(0.457 ± 0.076)
TYP

90° ± 4° TYP

(8.255 +1.016
−0.381)

0.100 ± 0.010
(2.54 ± 0.254)
TYP

N24C (REV F)

24-Lead (0.300″ Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)

0.090
0.060

0.040
0.030

0.625
0.590

0.050 ± 0.005

0.005 MIN TYP

24   13

0.370
0.250

0.420 MAX

0.015
0.008

0.019
0.015 TYP

0.015
0.008

0.370
0.250

SEE
DETAIL A

0.006
0.004

1   12

0.045 MAX

W24C (REV E)

24 Lead Ceramic Flatpak (F)
NS Package Number W24C

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.