National Semiconductor Corporation

DM54ALS645A/DM74ALS645A Octal Bus Transceivers

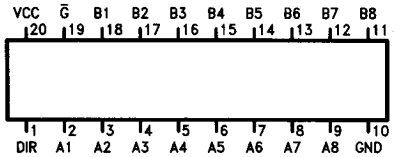
General Description

These octal bus transceivers are designed for asynchronous two-way communication between data busses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the busses are effectively isolated.

Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Switching performance specified at 50 pF
- PNP input design reduces input loading

Connection and Logic Diagrams



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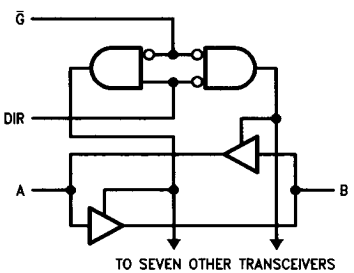
Order Number DM54ALS645AJ, DM74ALS645AWM or DM74ALS645AN
See NS Package Number J20A, M20B or N20A

'ALS645A



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Function Table

Control Inputs		Operation
$\bar{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

Low = Low Logic Level
High = High Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage; Control Inputs	7V
I/O ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS645A			DM74ALS645A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics Over Recommended Free Air Temperature Range

Symbol	Parameter	Test Conditions		DM54ALS645A			DM74ALS645A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5 to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = Max	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100			100	μA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 2)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 2)				−100			−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		30	48		30	45	mA
			Outputs Low		36	60		36	55	
			Outputs Disabled		38	63		38	58	

Note 2: For I/O ports, I_{IH} and I_{IL} parameters include the TRI-STATE® output current (I_{OZL} and I_{OZH}).

Switching Characteristics Over Recommended Operating Free Air Temperature Range

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54ALS645A		DM74ALS645A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B	B or A	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R1 = R2 = 500Ω (Note 1)	1	15	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B	B or A		1	13	3	10	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	A or B		2	30	5	20	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$	A or B		2	29	5	20	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	A or B		2	14	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$	A or B		2	30	4	15	ns

Note 1: See Section 1 for Test Waveforms and Output Load.