TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT74P, TC74ACT74F, TC74ACT74FN, TC74ACT74FT

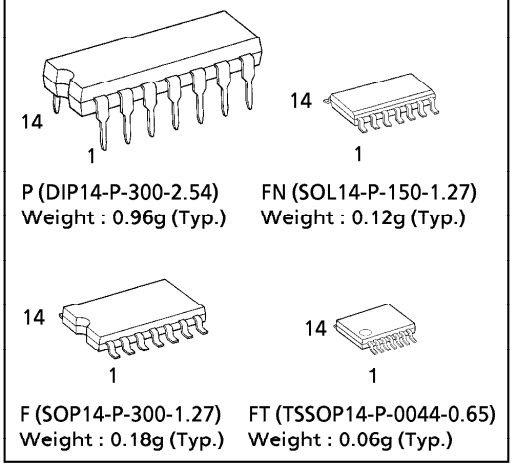
DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

The TC74ACT74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.
$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input to an "L" level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

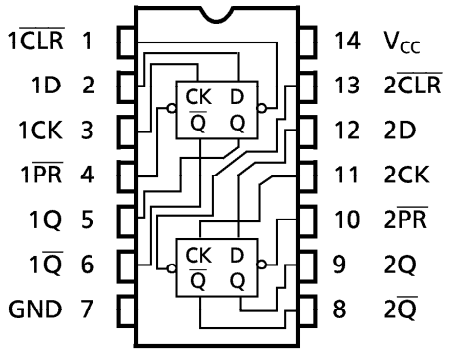
- High Speed ····· f_{MAX} = 180MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ··· V_{IL} = 0.8V (Max.), V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74F74

(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP14-P-300-2.54) Weight : 0.96g (Typ.)
FN (SOL14-P-150-1.27) Weight : 0.12g (Typ.)
F (SOP14-P-300-1.27) Weight : 0.18g (Typ.)
FT (TSSOP14-P-0044-0.65) Weight : 0.06g (Typ.)

PIN ASSIGNMENT

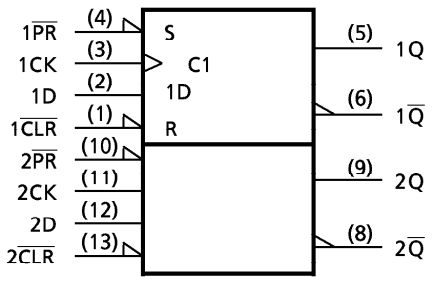


TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

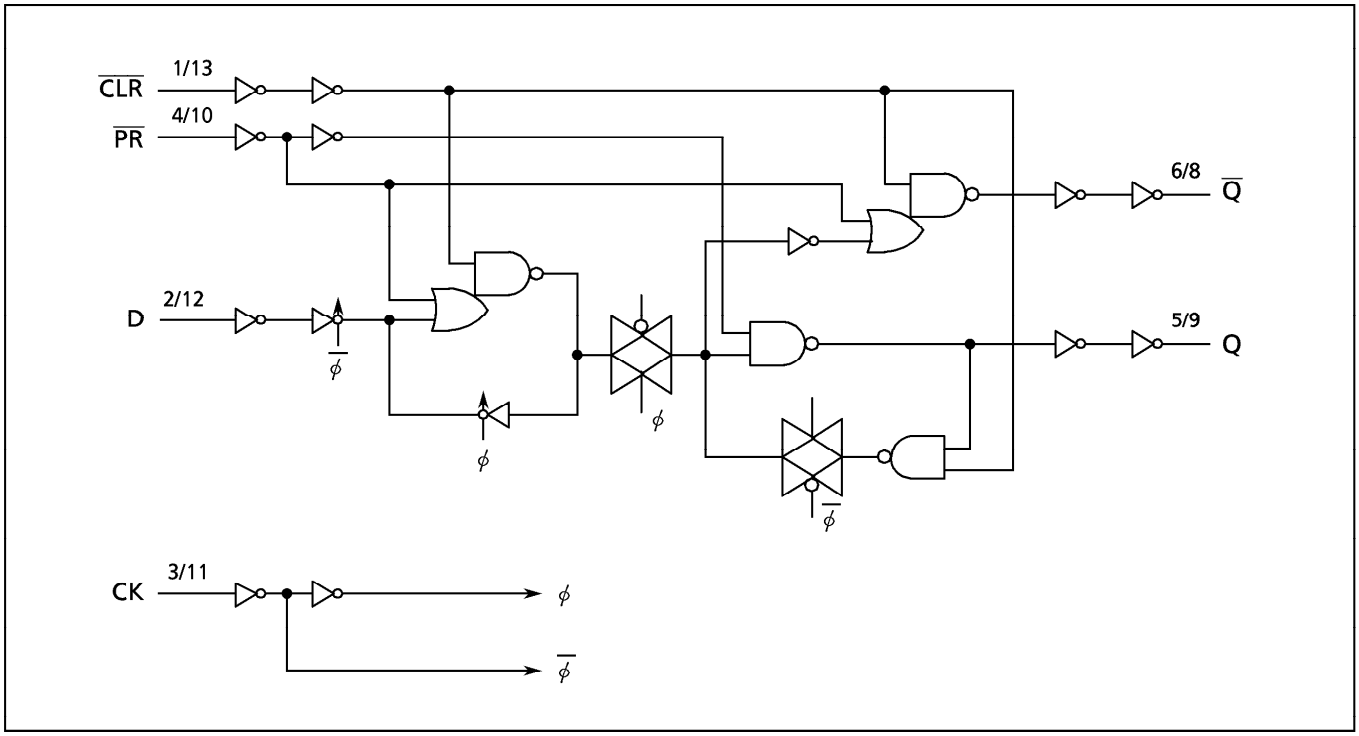
X : Don't Care

IEC LOGIC SYMBOL



961001EBA2

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75mA*	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	I_C	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta = 25°C	Ta = −40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0 ± 0.5	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		5.0 ± 0.5	5.7	6.5	
Minimum Set - up Time	t_s		5.0 ± 0.5	3.5	3.5	
Minimum Hold Time	t_h		5.0 ± 0.5	1.5	1.5	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		5.0 ± 0.5	2.0	2.0	

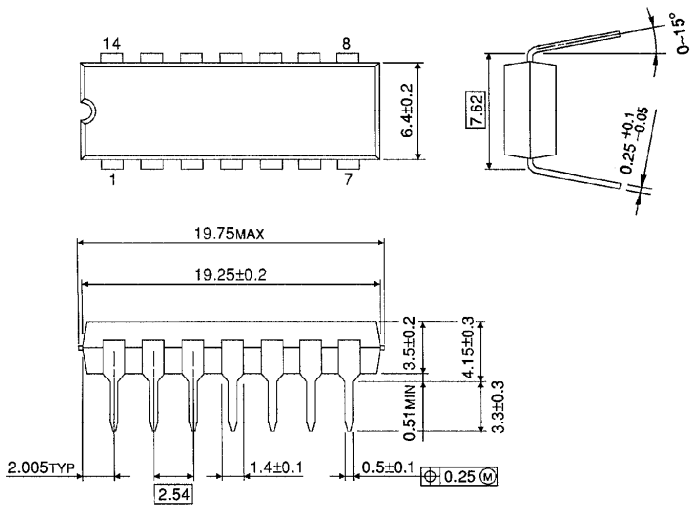
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF , R_L = 500 Ω , Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q , $\overline{Q}$)	t_{pLH} t_{pHL}		5.0 ± 0.5	−	6.1	9.2	1.0	10.5	ns
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q , $\overline{Q}$)	t_{pLH} t_{pHL}		5.0 ± 0.5	−	6.5	10.1	1.0	11.5	
Maximum Clock Frequency	f_{MAX}		5.0 ± 0.5	95	160	−	95	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)			−	35	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

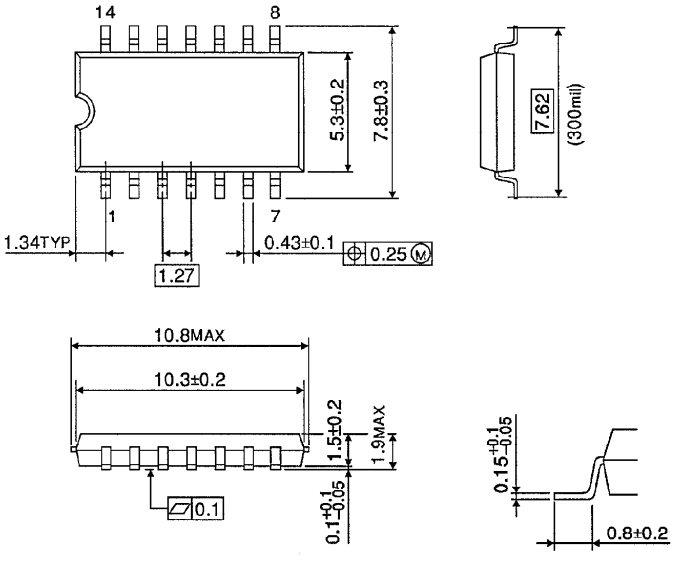
$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per F / F)}$$

DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54) Unit in mm



Weight : 0.96g (Typ.)

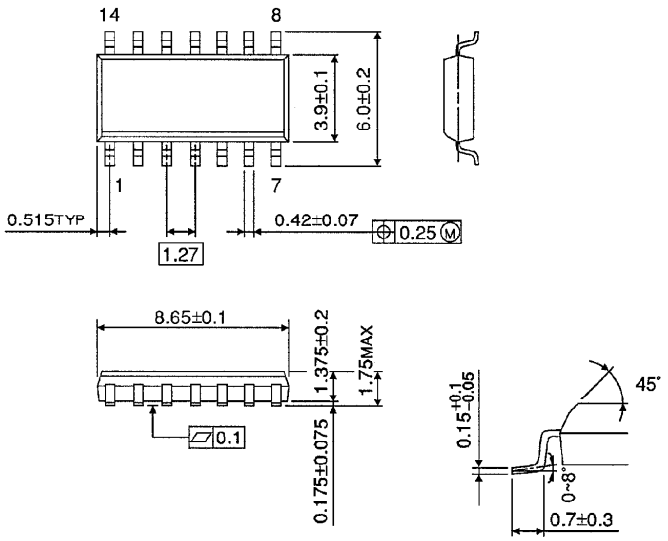
SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

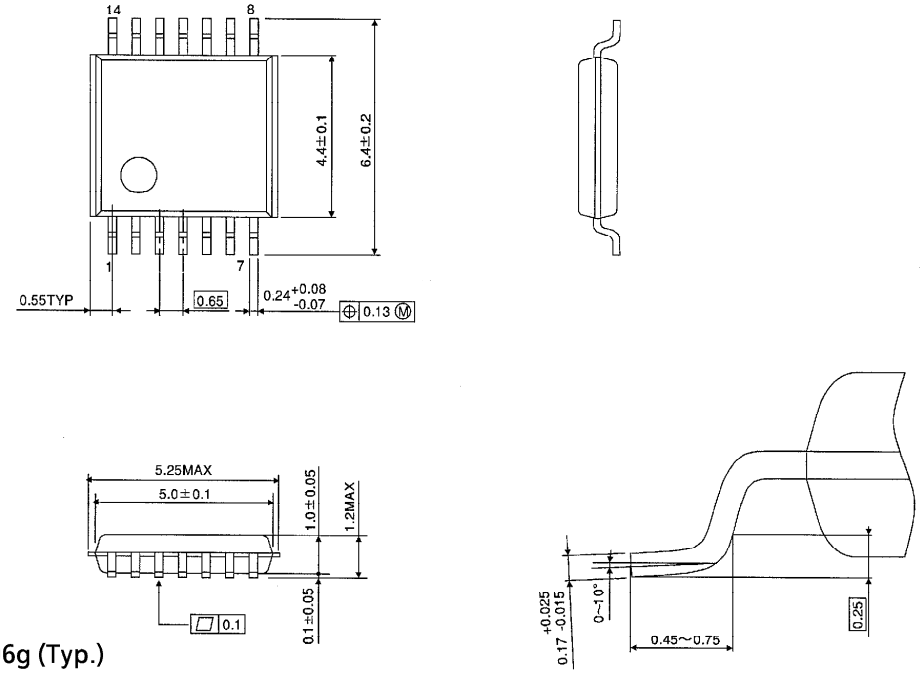
SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

TSSOP 14PIN (170mil BODY) OUTLINE DRAWING (TSSOP14-P-0044-0.65) Unit in mm



Weight : 0.06g (Typ.)