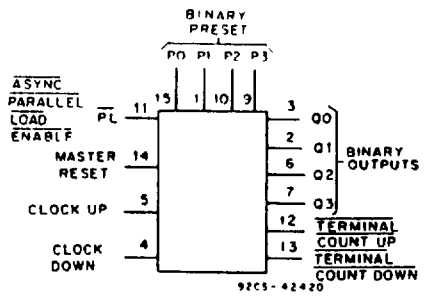
HARRIS SEMICONDUCTOR

NOT RECOMMENDED FOR NEW DESIGNS

Technical Data

CD54/74AC193
CD54/74ACT193

December 1997



FUNCTIONAL DIAGRAM

Presettable Synchronous 4-Bit Binary Up/Down Counter with Reset

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 11.2 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The Harris CD54/74AC193 and CD54/74ACT193 are up/down binary counters with separate up/down clocks. These devices use the Harris ADVANCED CMOS technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ($\overline{PL}$). The counter is incremented on the LOW-to-HIGH transition of the Clock-Up input (and a HIGH level on the Clock-Down input) and decremented on the LOW-to-HIGH transition of the Clock-Down input (and a HIGH level on the Clock-Up input). A HIGH level on the Reset input overrides any other input to clear the counter to its zero state. The $\overline{TCU}$ (carry) output goes LOW half a clock period before the zero count is reached and returns to a HIGH level at the zero count. The $\overline{TCD}$ (borrow) output in the count down mode likewise goes LOW half a clock period before the maximum count (15 counts) and returns to HIGH at the maximum count. Cascading is effected by connecting the $\overline{TCU}$ and $\overline{TCD}$ outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

The CD74AC/ACT193 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC193 and CD54ACT193, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - Drives 50-ohm transmission lines

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TRUTH TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FUNCTION
⎍	H	L	H	Count Up
H	⎍	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

H = High level
L = Low level
⎍ = Low-to-high transition
X = Don't care

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

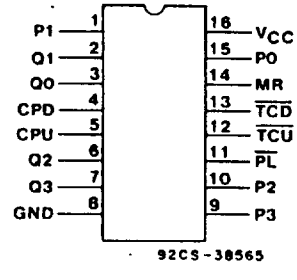
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT

CD54/74AC193
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STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
P0 - P3, $\overline{PL}$	0.75
MR, CPU, CPD	0.85

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width CPD	t_w	1.5	64	—	73	—	ns
		3.3*	7.1	—	8.1	—	
		5†	5.1	—	5.8	—	
$\overline{CPU}$	t_w	1.5	73	—	83	—	ns
		3.3	8.1	—	9.2	—	
		5	5.8	—	6.6	—	
$\overline{PL}$ Pulse Width	t_w	1.5	66	—	75	—	ns
		3.3	7.4	—	8.4	—	
		5	5.3	—	6	—	
MR Pulse Width	t_w	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
Recovery Time $\overline{PL}$ to CPU or CPD	t_{REC}	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
Recovery Time MR to CPU, CPD	t_{REC}	1.5	1	—	1	—	ns
		3.3	1	—	1	—	
		5	1	—	1	—	
Setup Time Pn to $\overline{PL}$	t_{su}	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	
Hold Time Pn to $\overline{PL}$	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Max. Frequency CPU	f_{max}	1.5	6.8	—	6	—	MHz
		3.3	62	—	54	—	
		5	86	—	75	—	
$\overline{CPD}$		1.5	7.8	—	6.8	—	MHz
		3.3	70	—	61	—	
		5	97	—	85	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

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SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: $\overline{PL}$ to Qn	t_{PLH}	1.5	—	171	—	188	ns
	t_{PHL}	3.3*	5.4	19.1	5.3	21	
		5†	3.9	13.6	3.8	15	
CPU to Qn CPD to Qn	t_{PLH}	1.5	—	159	—	175	ns
	t_{PHL}	3.3	5	17.8	4.9	19.6	
		5	3.6	12.7	3.5	14	
CPU to $\overline{TCU}$ CPD to $\overline{TCD}$	t_{PLH}	1.5	—	127	—	140	ns
	t_{PHL}	3.3	4	14.3	3.9	15.7	
		5	2.9	10.2	2.8	11.2	
MR to Qn	t_{PLH}	1.5	—	182	—	200	ns
	t_{PHL}	3.3	5.8	20.4	5.6	22.4	
		5	4.1	14.5	4	16	
MR to $\overline{TCU}$	t_{PLH}	1.5	—	171	—	188	ns
	t_{PHL}	3.3	5.5	19.1	5.3	21	
		5	3.9	13.6	3.8	15	
MR to $\overline{TCD}$	t_{PLH}	1.5	—	207	—	228	ns
	t_{PHL}	3.3	6.6	23.2	6.4	25.5	
		5	4.7	16.5	4.6	18.2	
Pn to Qn	t_{PLH}	1.5	—	187	—	206	ns
	t_{PHL}	3.3	5.9	21	5.8	23.1	
		5	4.2	15	4.1	16.5	
Power Dissipation Capacitance	C_{PD}§	—	95 Typ.		95 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width: CPU	t_w	5†	6.8	—	7.7	—	ns
CPD			5.8	—	6.6	—	
$\overline{PL}$ Pulse Width	t_w	5	6.6	—	7.5	—	ns
MR Pulse Width	t_w	5	4.4	—	5	—	ns
Recovery Time: $\overline{PL}$ to CPU or CPD	t_{REC}	5	5.7	—	6.5	—	ns
MR to CPU, CPD			1	—	1	—	
Setup Time Pn to $\overline{PL}$	t_{SU}	5	4.7	—	5.4	—	ns
Hold Time Pn to $\overline{PL}$	t_H	5	2	—	2	—	ns
Max. Frequency: CPU	f_{max}	5	74	—	65	—	MHz
CPD			86	—	75	—	

†5V min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: $\overline{PL}$ to Qn	t_{PLH} t_{PHL}	5†	3.9	13.6	3.8	15	ns
CPU to Qn		5	3.6	12.7	3.5	14	
CPD to Qn		5	3.6	12.7	3.5	14	
CPU to $\overline{TCU}$		5	2.9	10.2	2.8	11.2	
CPD to $\overline{TCD}$		5	2.9	10.2	2.8	11.2	
MR to Qn		5	4.1	14.5	4	16	
MR to $\overline{TCU}$		5	3.9	13.6	3.8	15	
MR to $\overline{TCD}$		5	4.7	16.5	4.6	18.2	
Pn to Qn		5	4.2	15	4.1	16.5	
Power Dissipation Capacitance	C_{PD}§	—	95 Typ.		95 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

†5V: min. is @ 5.5 V
max. is @ 4.5 V.

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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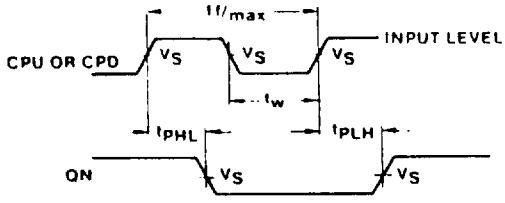
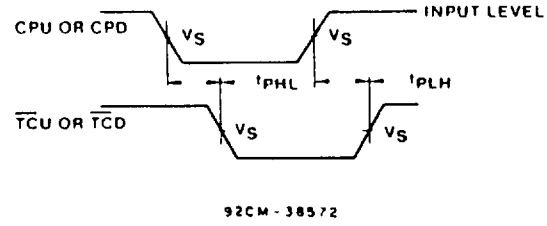
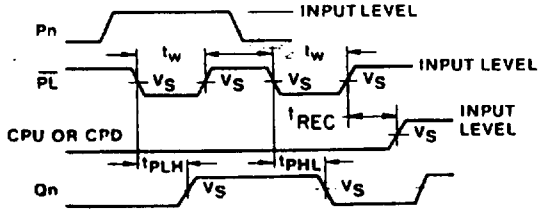


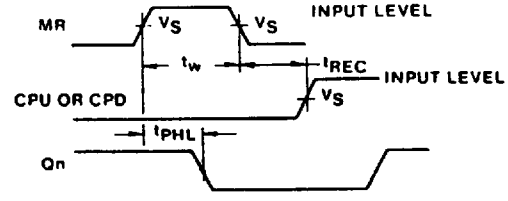
(a) Clock to output delays and clock pulse width.



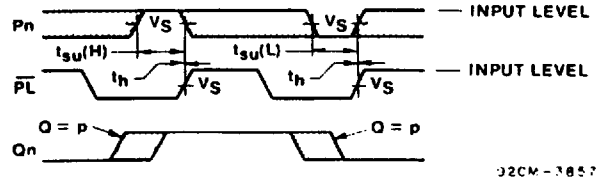
(b) Clock to terminal count delays.



(c) Parallel load pulse width, parallel load to output delays, and parallel load to clock recovery time.



(d) Master reset pulse width, master reset to output delay and master reset to clock recovery time.

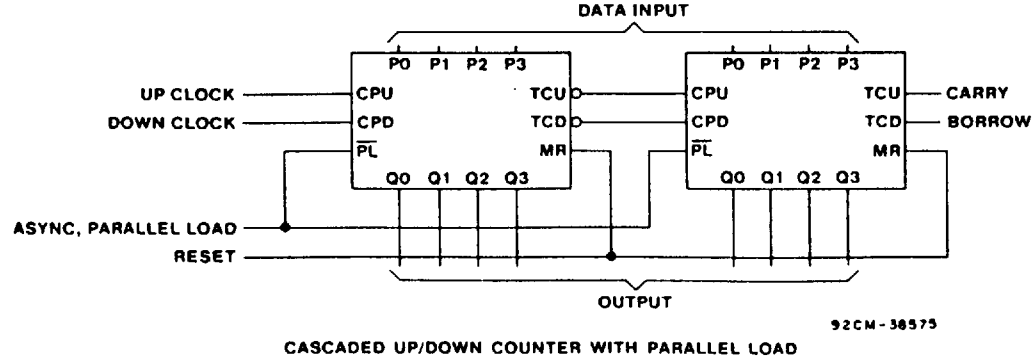


(e) Setup and hold times data to parallel load (PL).

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - AC waveforms.

APPLICATION



CASCADED UP/DOWN COUNTER WITH PARALLEL LOAD

Sequences:
(1) Reset outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, terminal count up, zero, one and two.
(4) Count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

Note 1: Master reset overrides load data and clock inputs
Note 2: When counting up, clock-down input must be high; when counting down, clock-up input must be high.

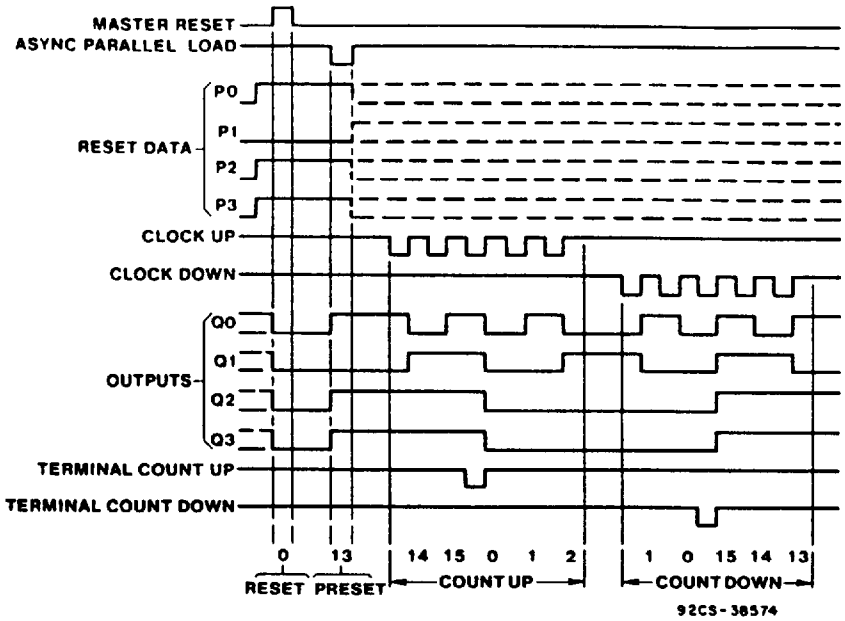


Fig. 2 - Timing diagram.