TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74AC574P,TC74AC574F,TC74AC574FT

## Octal D-Type Flip-Flop with 3-State Output

The TC74AC574 is an advanced high speed CMOS OCTAL FLIP-FLOP fabricated with silicon gate and double-layer metal wiring $C^2MOS$ technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

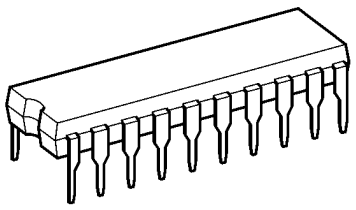
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

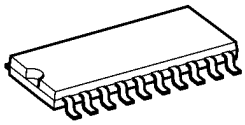
- High speed: $f_{max}$ = 180 MHz (typ.) at $V_{CC}$ = 5 V
- Low power dissipation: $I_{CC}$ = 8 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2 to 5.5 V
- Pin and function compatible with 74F574

TC74AC574P



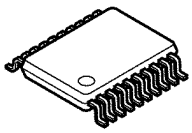
DIP20-P-300-2.54A

TC74AC574F



SOP20-P-300-1.27A

TC74AC574FT

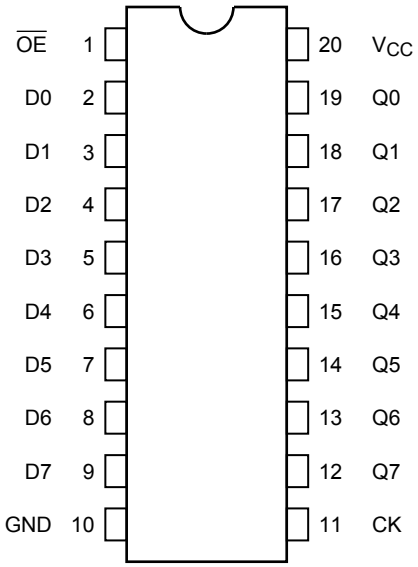


TSSOP20-P-0044-0.65A

Weight

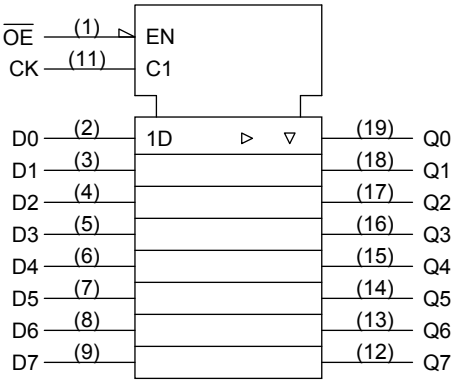
| | |
|---|---|
| DIP20-P-300-2.54A | : 1.30 g (typ.) |
| SOP20-P-300-1.27A | : 0.22 g (typ.) |
| TSSOP20-P-0044-0.65A | : 0.08 g (typ.) |

## Pin Assignment




(top view)

## IEC Logic Symbol




## Truth Table

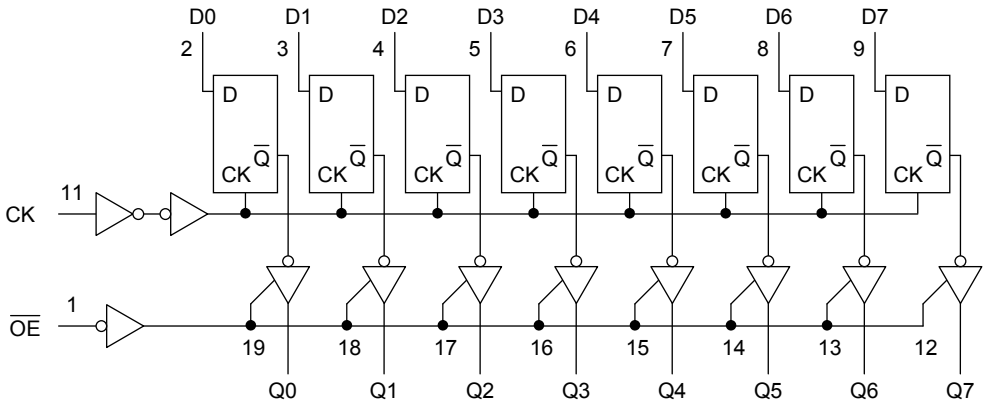
| Inputs | | | Output |
|---|---|---|---|
| $\overline{OE}$ | CK | D | Q |
| H | X | X | Z |
| L | ↓ | X | $Q_n$ |
| L | ↑ | L | L |
| L | ↑ | H | H |

X: Don't care

Z: High impedance

$Q_n$: No change

## System Diagram



## Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7.0 | V |
| DC input voltage | $V_{IN}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | ±20 | mA |
| Output diode current | $I_{OK}$ | ±50 | mA |
| DC output current | $I_{OUT}$ | ±50 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±200 | mA |
| Power dissipation | $P_D$ | 500 (DIP) (Note 2)/180 (SOP/TSSOP) | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.0 to 5.5 | V |
| Input voltage | $V_{IN}$ | 0 to $V_{CC}$ | V |
| Output voltage | $V_{OUT}$ | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time | dt/dV | 0 to 100 ($V_{CC}$ = 3.3 ± 0.3 V)<br>0 to 20 ($V_{CC}$ = 5 ± 0.5 V) | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Ta = 25°C Min | Ta = 25°C Typ. | Ta = 25°C Max | Ta = −40 to 85°C Min | Ta = −40 to 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | — | 1.50 | — | V |
| | | | | 3.0 | 2.10 | — | — | 2.10 | — | |
| | | | | 5.5 | 3.85 | — | — | 3.85 | — | |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | — | 0.50 | — | 0.50 | V |
| | | | | 3.0 | — | — | 0.90 | — | 0.90 | |
| | | | | 5.5 | — | — | 1.65 | — | 1.65 | |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | $I_{OH}$ = −4 mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | $I_{OH}$ = −24 mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| | | | $I_{OH}$ = −75 mA (Note) | 5.5 | — | — | — | 3.85 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL}$ = 12 mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 24 mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 75 mA (Note) | 5.5 | — | — | — | — | 1.65 | |
| 3-state output off-state current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.5 | — | ±5.0 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 8.0 | — | 80.0 | μA |

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

### Timing Requirements (input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Ta = 25°C Limit | Ta = −40 to 85°C Limit | Unit |
|---|---|---|---|---|---|---|
| Minimum pulse width (CK) | $t_{w\,(H)}$ | — | 3.3 ± 0.3 | 7.0 | 7.0 | ns |
| | $t_{w\,(L)}$ | | 5.0 ± 0.5 | 5.0 | 5.0 | |
| Minimum set-up time | $t_s$ | — | 3.3 ± 0.3 | 9.0 | 9.0 | ns |
| | | | 5.0 ± 0.5 | 4.5 | 4.5 | |
| Minimum hold time | $t_h$ | — | 3.3 ± 0.3 | 1.0 | 1.0 | ns |
| | | | 5.0 ± 0.5 | 1.0 | 1.0 | |

**AC Characteristics ($C_L$ = 50 pF, $R_L$ = 500 Ω, input: $t_r = t_f$ = 3 ns)**

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Min | Typ. | Max | Min | Max | |
| Propagation delay time (CK-Q) | $t_{pLH}$ | — | 3.3 ± 0.3 | — | 9.8 | 16.7 | 1.0 | 19.0 | ns |
| | $t_{pHL}$ | | 5.0 ± 0.5 | — | 6.1 | 9.2 | 1.0 | 10.5 | |
| Output enable time | $t_{pZL}$ | — | 3.3 ± 0.3 | — | 9.2 | 15.8 | 1.0 | 18.0 | ns |
| | $t_{pZH}$ | | 5.0 ± 0.5 | — | 6.1 | 9.3 | 1.0 | 10.6 | |
| Output disable time | $t_{pLZ}$ | — | 3.3 ± 0.3 | — | 6.6 | 11.0 | 1.0 | 12.5 | ns |
| | $t_{pHZ}$ | | 5.0 ± 0.5 | — | 5.8 | 8.8 | 1.0 | 10.0 | |
| Maximum clock frequency | $f_{max}$ | — | 3.3 ± 0.3 | 50 | 100 | — | 50 | — | MHz |
| | | | 5.0 ± 0.5 | 95 | 160 | — | 95 | — | |
| Input capacitance | $C_{IN}$ | — | | — | 5 | 10 | — | 10 | pF |
| Output capacitance | $C_{OUT}$ | — | | — | 10 | — | — | — | pF |
| Power dissipation capacitance | $C_{PD}$ | (Note) | | — | 36 | — | — | — | pF |

Note: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

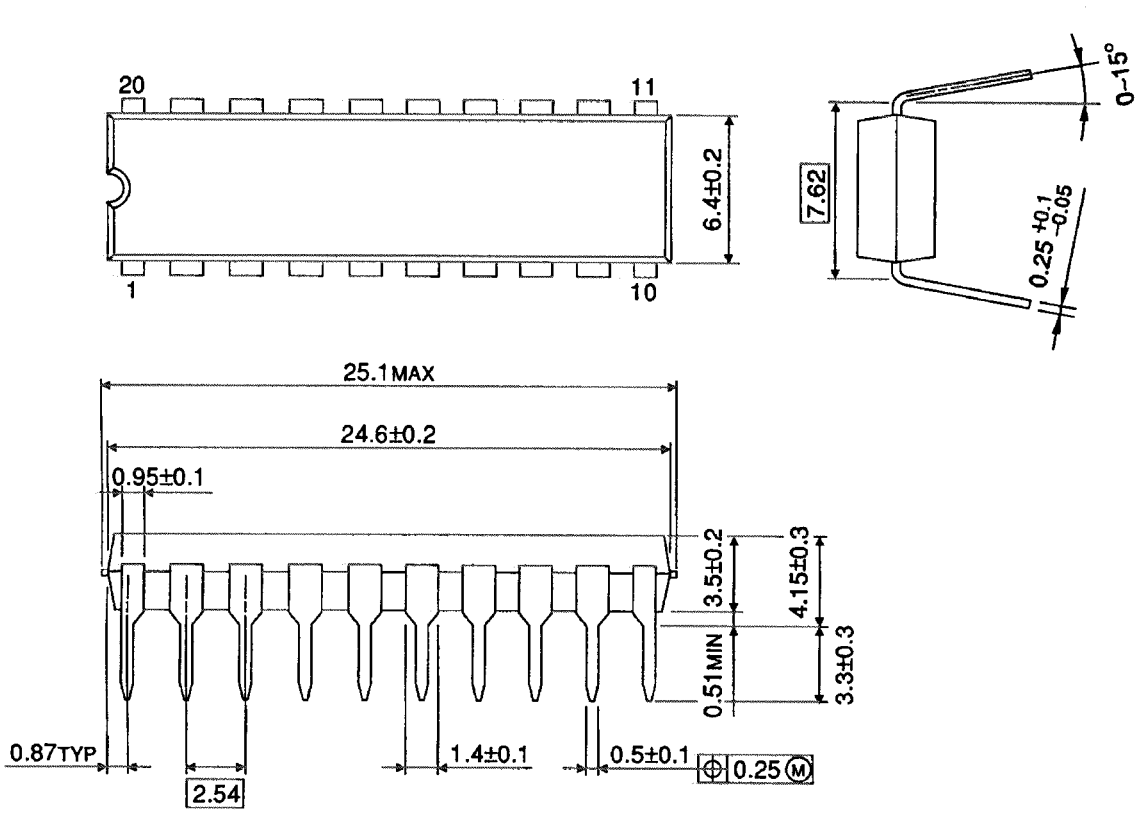
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F)

And the total $C_{PD}$ when n pcs. of latch operate can be gained by the following equation:

$C_{PD}$ (total) = 26 + 10·n

## Package Dimensions

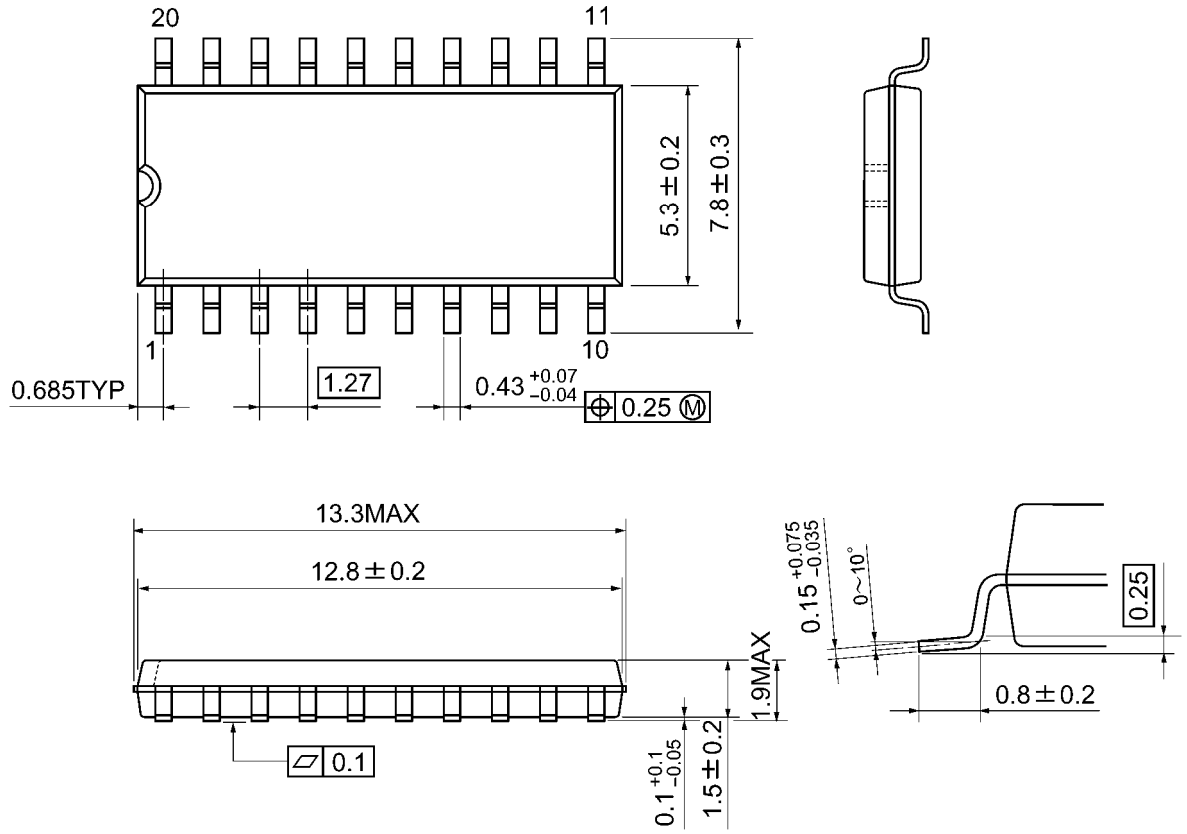
DIP20-P-300-2.54A Unit : mm




Weight: 1.30 g (typ.)

## Package Dimensions

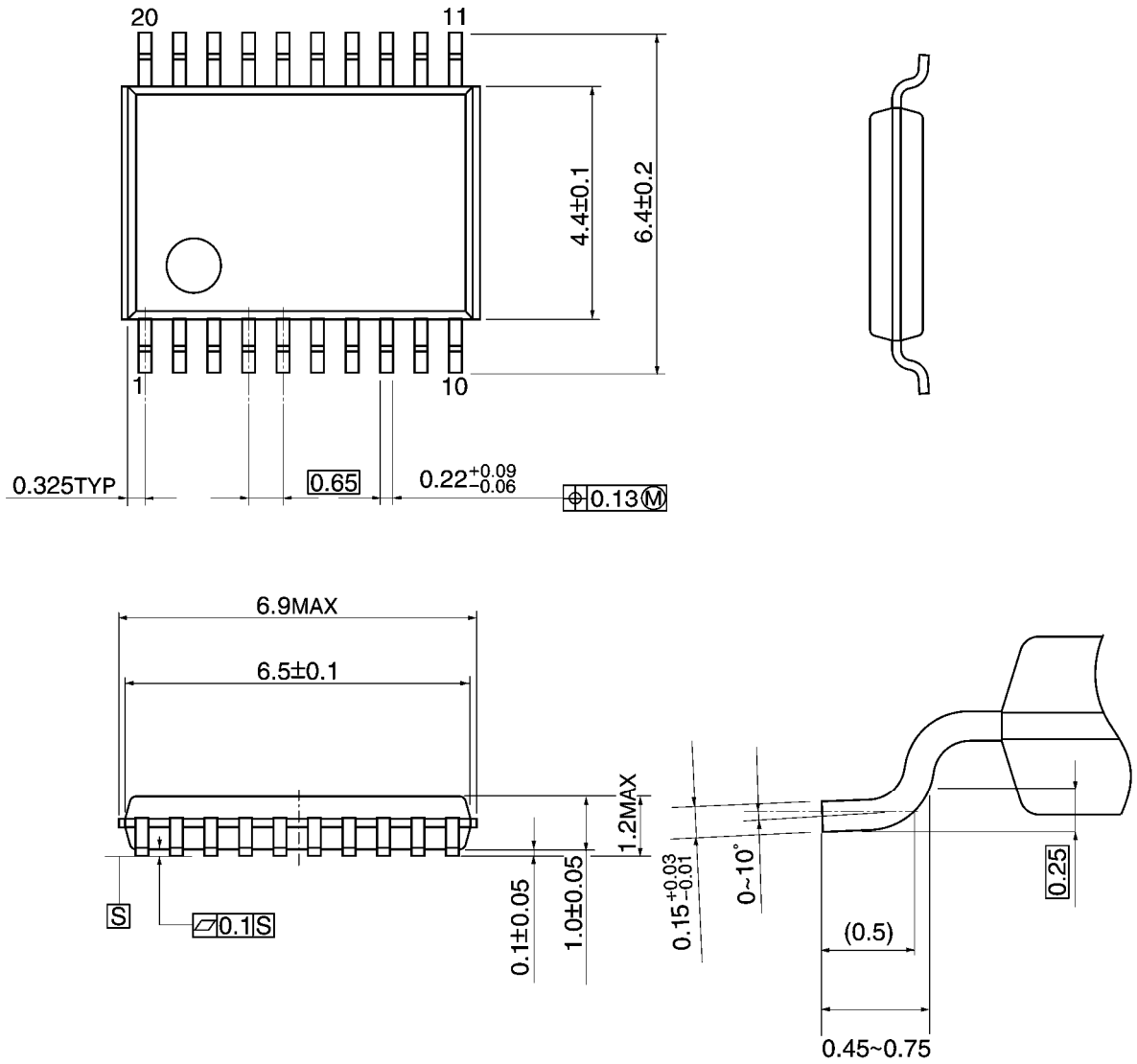
SOP20-P-300-1.27A Unit: mm




Weight: 0.22 g (typ.)

## Package Dimensions

TSSOP20-P-0044-0.65A Unit: mm




Weight: 0.08 g (typ.)

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