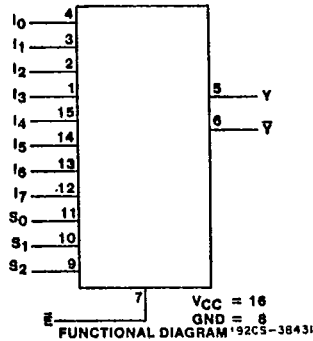


**CD54/74AC151**  
**CD54/74ACT151**

T-67-21-51

Advance Information



**8-Input Multiplexer**

- Type Features:**
- Buffered inputs
  - Typical propagation delay:  
6 ns @  $V_{CC} = 5V, T_A = 25^\circ C, C_L = 50 pF$

**Family Features:**

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

The RCA CD54/74AC151 and CD54/74ACT151 8-input digital multiplexers use the RCA ADVANCED CMOS technology. They have three binary control inputs (S0, S1, and S2) and an active-LOW Enable ( $\bar{E}$ ) input. The three binary inputs select 1 of 8 channels. The output is both inverting ( $\bar{Y}$ ) and non inverting (Y).

The CD74AC151 and CD74ACT151 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC151 and CD54ACT151, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

INPUTS												OUTPUTS	
$\bar{E}$	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>	I <sub>5</sub>	I <sub>6</sub>	I <sub>7</sub>	$\bar{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	H	X	X	X	X	H	X	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	H	X	X	X	X	X	X	H	X	L	H
L	H	H	L	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	L	H	L

H = HIGH voltage level. L = LOW voltage level. X = Don't care.



T-67-21-51

Technical Data

**CD54/74AC151**  
**CD54/74ACT151**

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE ( $V_{CC}$ )	.....	-0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{IK}$ (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	.....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_O$ (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	.....	$\pm 50$ mA
DC $V_{CC}$ or GROUND CURRENT ( $I_{CC}$ or $I_{GND}$ )	.....	$\pm 100$ mA*
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	.....	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	.....	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	.....	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	.....	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	.....	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE ( $T_{STG}$ )	.....	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s maximum	.....	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. ( $1.59$ mm) with solder contacting lead tips only	.....	$+300^\circ\text{C}$

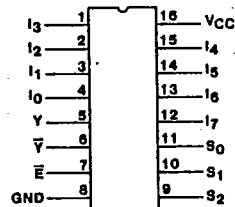
\*For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A =$ Full Package-Temperature Range) AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I, V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$ at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



92CS-38432

**TERMINAL ASSIGNMENT**

T-67-21-51 CD54/74AC151  
CD54/74ACT151

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, *	-0.05	1.5	1.4	—	1.4	—	1.4	V	
			-0.05	3	2.9	—	2.9	—	2.9		
			-0.05	4.5	4.4	—	4.4	—	4.4		
			-4	3	2.58	—	2.48	—	2.4		
			-24	4.5	3.94	—	3.8	—	3.7		
			-75	5.5	—	—	3.85	—	—		
			-50	5.5	—	—	—	—	3.85		
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, *	0.05	1.5	—	0.1	—	0.1	—	V	
			0.05	3	—	0.1	—	0.1	—		
			0.05	4.5	—	0.1	—	0.1	—		
			12	3	—	0.36	—	0.44	—		0.5
			24	4.5	—	0.36	—	0.44	—		0.5
			75	5.5	—	—	—	1.65	—		—
			50	5.5	—	—	—	—	—		1.65
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MS <sub>I</sub> I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.  
\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.



Technical Data

**CD54/74AC151**  
**CD54/74ACT151**

T-67-21-51

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS	$V_{CC}$ (V)	AMBIENT TEMPERATURE ( $T_A$ ) - °C						UNITS		
			+25		-40 to +85		-55 to +125				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
High-Level Input Voltage	$V_{IH}$		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	$V_{IL}$		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$ #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$ #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	$I_I$	$V_{CC}$ or GND	5.5	—	±0.1	—	±1	—	±1	µA	
Quiescent Supply Current, MSI	$I_{CC}$	$V_{CC}$ or GND	0	5.5	—	8	—	80	—	160	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}-2.1$	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
I (All)	1
E	1
S	1

\*Unit load is  $\Delta I_{CC}$  limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data  
**CD54/74AC151**  
**CD54/74ACT151**

T-67-21-51

SWITCHING CHARACTERISTICS: AC Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Data to Y	t <sub>PLH</sub>	1.5	—	152	—	169	ns
	t <sub>PHL</sub>	3.3*	4.9	17.1	4.7	18.9	
		5†	3.5	12.3	3.4	13.5	
Any Data to $\bar{Y}$	t <sub>PLH</sub>	1.5	—	169	—	186	ns
	t <sub>PHL</sub>	3.3	5.4	19	5.2	20.9	
		5	3.8	13.5	3.7	14.9	
Any Select to Y	t <sub>PLH</sub>	1.5	—	207	—	228	ns
	t <sub>PHL</sub>	3.3	6.6	23.2	6.4	25.5	
		5	4.7	16.5	4.6	18.2	
Any Select to $\bar{Y}$	t <sub>PLH</sub>	1.5	—	223	—	245	ns
	t <sub>PHL</sub>	3.3	7.1	24.9	6.9	27.4	
		5	5.1	17.8	4.9	19.6	
Any Enable to Y	t <sub>PLH</sub>	1.5	—	139	—	153	ns
	t <sub>PHL</sub>	3.3	4.4	15.5	4.3	17.1	
		5	3.1	11.1	3.1	12.2	
Any Enable to $\bar{Y}$	t <sub>PLH</sub>	1.5	—	153	—	169	ns
	t <sub>PHL</sub>	3.3	4.9	17.2	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	120 Typ.		120 Typ.		pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*3.3 V: min. is @ 3.6 V  
 max. is @ 3 V  
 †5 V: min. is @ 5.5 V  
 max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per device.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.

SWITCHING CHARACTERISTICS: ACT Series;  $t_r, t_f = 3 \text{ ns}$ ,  $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Data to Y	t <sub>PLH</sub>	5*	4	14.1	3.9	15.5	ns
	t <sub>PHL</sub>						
Any Data to $\bar{Y}$	t <sub>PLH</sub>	5	4.4	15.4	4.2	16.9	ns
	t <sub>PHL</sub>						
Any Select to Y	t <sub>PLH</sub>	5	5.2	18.4	5.1	20.2	ns
	t <sub>PHL</sub>						
Any Select to $\bar{Y}$	t <sub>PLH</sub>	5	5.6	19.6	5.4	21.6	ns
	t <sub>PHL</sub>						
Any Enable to Y	t <sub>PLH</sub>	5	3.1	11	3	12.1	ns
	t <sub>PHL</sub>						
Any Enable to $\bar{Y}$	t <sub>PLH</sub>	5	3.5	12.3	3.4	13.5	ns
	t <sub>PHL</sub>						
Power Dissipation Capacitance	C <sub>PD</sub> §	—	120 Typ.		120 Typ.		pF
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF

\*5 V: min. is @ 5.5 V  
 max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency  
 $C_L$  = output load capacitance  
 $V_{CC}$  = supply voltage.



Technical Data

**CD54/74AC151**  
**CD54/74ACT151**

T-67-21-51

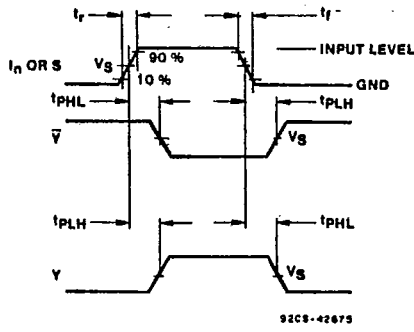


Fig. 1 - Inputs or select to output propagation delays.

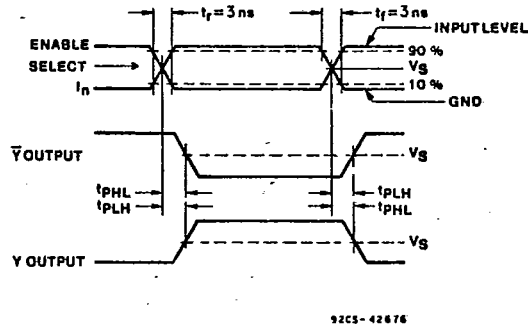


Fig. 2 - Enable to output propagation delays.

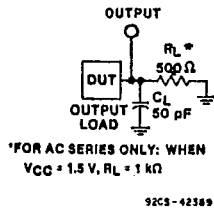
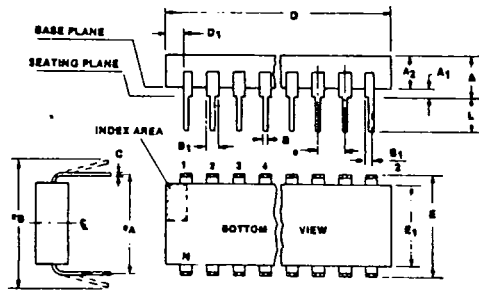


Fig. 3 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V <sub>CC</sub>	3 V
Input Switching Voltage, V <sub>s</sub>	0.5 V <sub>CC</sub>	1.5 V
Output Switching Voltage, V <sub>s</sub>	0.5 V <sub>CC</sub>	0.5 V <sub>CC</sub>

Dual-In-Line Plastic Packages

T-90-20



Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions  $1, N, \frac{N}{2}, \frac{N}{2} + 1$ .
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E<sub>1</sub> does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e<sub>A</sub>.
10. e<sub>B</sub> is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D<sub>1</sub> at the left end of the package must equal dimension D<sub>1</sub> at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

(E) Suffix (JEDEC MS-001-AC)  
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B <sub>1</sub>	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)  
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B <sub>1</sub>	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

(E) Suffix (JEDEC MS-001-AE)  
20-Lead Dual-In-Line Plastic Package

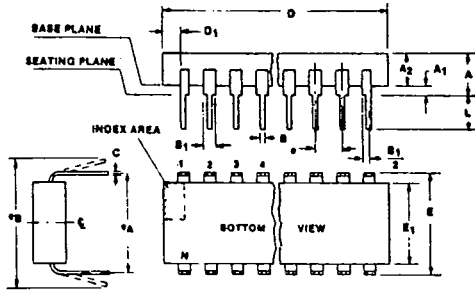
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B <sub>1</sub>	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

# Dual-In-Line Plastic Packages

## T-90-20

(E) Suffix (JEDEC MS-001-AF)  
24-Lead Dual-In-Line Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A <sub>1</sub>	0.015	—	0.39	—	9
A <sub>2</sub>	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B <sub>1</sub>	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D <sub>1</sub>	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E <sub>1</sub>	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e <sub>A</sub>	0.300 BSC		7.62 BSC		9
e <sub>B</sub>	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

**Notes:**

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions  

$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E<sub>1</sub> does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around

center line shown in end view.

8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e<sub>A</sub>.
10. e<sub>B</sub> is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D<sub>1</sub> at the left end of the package must equal dimension D<sub>1</sub> at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

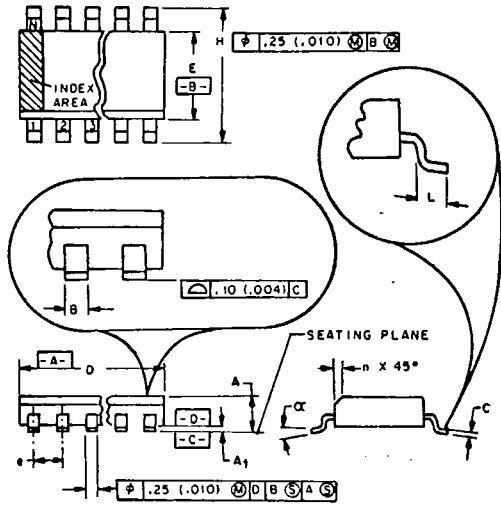




Dimensional Outlines

# Dual-In-Line Small-Outline Plastic Packages

T-90-20



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

M Suffix (JEDEC MS-012AB)  
14-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A <sub>1</sub>	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0° 8°		0° 8°		

Notes: 1, 2, 3, 8, 9

92CS-38924R2

M Suffix (JEDEC MS-012AC)  
16-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A <sub>1</sub>	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0° 8°		0° 8°		

Notes: 1, 2, 3, 8, 9

92CS-38925R2

M Suffix (JEDEC MS-013AC)  
20-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A <sub>1</sub>	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4861	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0° 8°		0° 8°		

Notes: 1, 2, 3, 8, 9

92CS-38926R2

M Suffix (JEDEC MS-013AD)  
24-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A <sub>1</sub>	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0° 8°		0° 8°		

Notes: 1, 2, 3, 8, 9

92CS-39037R2