

SN54120, SN74120 DUAL PULSE SYNCHRONIZERS/DRIVERS

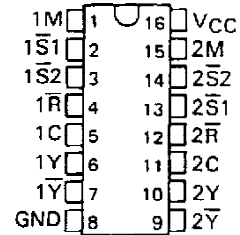
SDLS041

SEPTEMBER 1971 — REVISED MARCH 1988

- Generates Either a Single Pulse or Train of Pulses Synchronized with Control Functions
- Ideal for Implementing Sync-Control Circuits Similar to those Used in Oscilloscopes
- Latched Operation Ensures that Output Pulses Are Not Clipped
- High-Fan-Out Complementary Outputs Drive System Clock Lines Directly
- Internal Input Pull-Up Resistors Eliminate Need for External Components
- Diode-Clamped Inputs Simplify System Design
- Typical Propagation Delays:

9 Nanoseconds through One Level
16 Nanoseconds through Two Levels

SN54120 . . . J PACKAGE
SN74120 . . . N PACKAGE
(TOP VIEW)



description

These monolithic pulse synchronizers are designed to synchronize an asynchronous or manual signal with a system clock. Reliable response is ensured as the input signals are latched up; therefore duration of logic input is not critical and the adverse effects of contact-bounce of a manual input are eliminated. The ability to pass output pulses is started and stopped by the levels or pulses applied to the latch inputs $\bar{S}1$, $\bar{S}2$, or \bar{R} in accordance with the function table. High-speed circuitry is utilized throughout the clock paths to minimize skew with respect to the system clock.

After initiation, the mode control (M) input determines whether a series of pulses or only one pulse is passed. In the absence of a stop command, the clock driver will continue to pass clock pulses as long as the mode control input is low (see Figures 2 through 4). After the mode control input is taken high, only a single clock pulse will be passed (see Figure 5).

When the mode control is set to pass a series of pulses, the last pulse out is determined by two general rules:

- a. When pulses are terminated by the \bar{S} or \bar{R} inputs, conditions meeting the setup times (specified under recommended operating conditions) will dominate.
- b. Low-to-high-level transitions at the mode control input should be avoided during the 20-nanosecond period immediately following the negative transition of the input clock pulse as transitions during this time period may or may not allow the next pulse to pass (see Figures 4 and 5). When pulses are terminated by the mode control input, a positive transition at the mode control input meeting the high-level setup time, $t_{SU}(H)$, (specified under recommended operating conditions) will pass that positive clock pulse then inhibit remaining clock pulses. The clock input (C) is latch-controlled ensuring that once initiated the output pulse will not be terminated until the full pulse has been passed.

FUNCTION TABLE

INPUTS			FUNCTION
\bar{R}	$\bar{S}1$	$\bar{S}2$	
X	L	X	Pass Output Pulses
X	X	L	Pass Output Pulses
L	H	H	Inhibit Output Pulses
H	↓	H	Start Output Pulses
H	H	↓	Start Output Pulses
↓	H	H	Stop Output Pulses
H	H	H	Continue†

H = high level (steady state)

L = low level (steady state)

↓ = transition from H to L

X = irrelevant

† Operation initiated by last ↓ transition continues.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.


**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

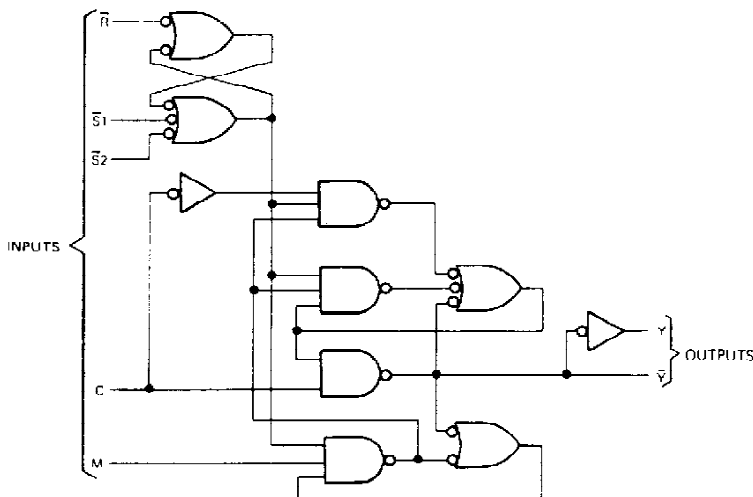
SN54120, SN74120 DUAL PULSE SYNCHRONIZERS/DRIVERS

description (continued)

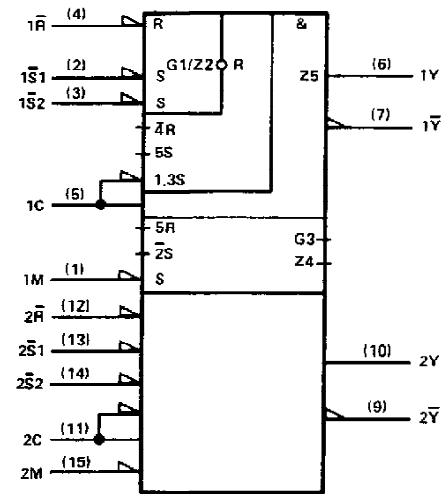
This clock driver circuit is entirely compatible for use with either digital logic circuits or mechanical switches for input controls since all inputs, except the clock, have internal pull-up resistors. This eliminates the requirement to supply an external resistor to prevent the input from floating when the control switch is open. The internal resistor also means that these inputs may be left disconnected if unused.

Typical propagation delay time is 9 nanoseconds to the \bar{Y} output and 16 nanoseconds to the Y output from the clock input. The outputs will drive 60 Series 54/74 loads at a high logic level and 30 loads at a low logic level. Typical power dissipation is 127 milliwatts per driver. The SN54120 is characterized for operation from -55°C to 125°C ; the SN74120 is characterized for operation from 0°C to 70°C .

logic diagram (each driver) (positive logic)

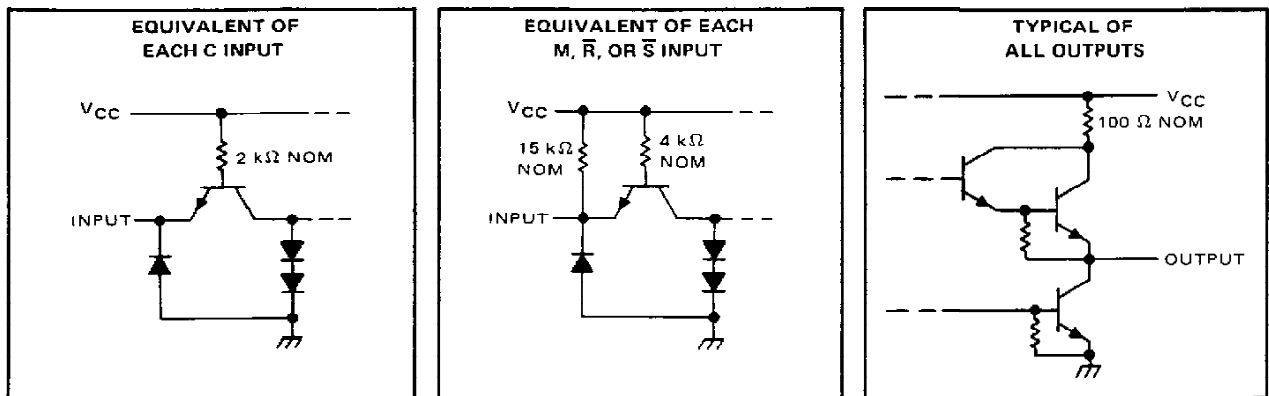


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



SN54120, SN74120 DUAL PULSE SYNCHRONIZERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54120 Circuits	-55°C to 125°C
SN74120 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the S1 and S2 inputs.

recommended operating conditions

		SN54120			SN74120			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}				-2.4			-2.4	mA	
Low-level output current, I_{OL}				48			48	mA	
Setup time (see Figures 2 thru 5)	Any input except mode control, $t_{su}(H \text{ or } L)$	12			12			ns	
	Mode control	$t_{su}(H)$	0			0			
		$t_{su}(L)$	12			12			
Hold time (see Figures 3 and 5)	Any input except mode control, $t_h(H \text{ or } L)$	3			3			ns	
	Mode control, $t_h(H \text{ or } L)$	20			20				
Operating free-air temperature, T_A		-55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT	
V_{IH}	High-level input voltage		2			V	
V_{IL}	Low-level input voltage				0.8	V	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -2.4 \text{ mA}$	2.4	3.4		V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 48 \text{ mA}$		0.2	0.4	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA	
I_{IH}	High-level input current	Clock input			80	μA	
		Other inputs	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$	-0.12	-0.2	-0.36	mA
I_{IL}	Low-level input current	Clock input			-3.2	mA	
		Other inputs	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-2.1	mA
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$			-35	-90	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$. See Note 3			51	90	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with ground applied to all inputs except R which is at 4.5 V and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C	Y	$C_L = 45 \text{ pF}$, $R_L = 133 \Omega$, See Figure 1	14		22	ns
t_{PHL}				17		25	
t_{PLH}	C	\bar{Y}		10		16	ns
t_{PHL}				8		13	

[¶] t_{PLH} = Propagation delay time, low-to-high-level output

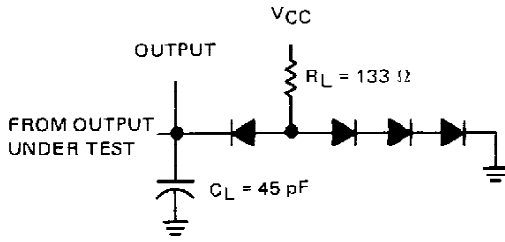
t_{PHL} = Propagation delay time, high-to-low-level output


**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

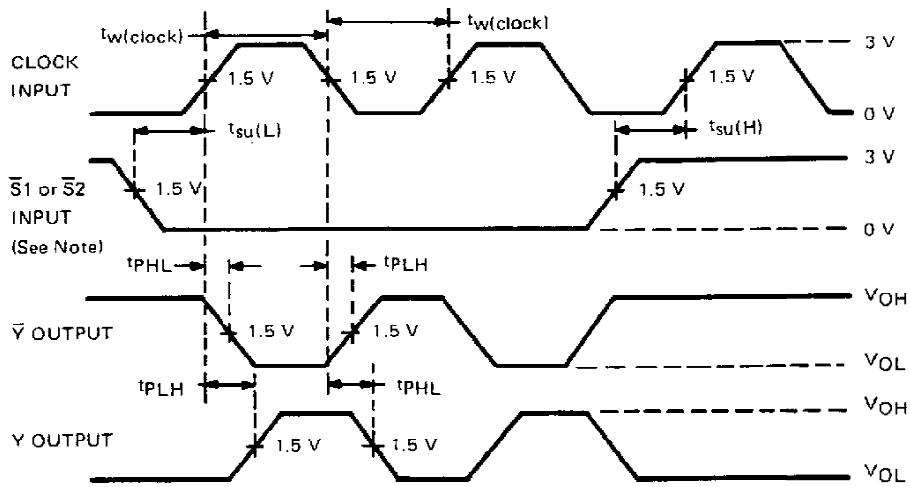
SN54120, SN74120
DUAL PULSE SYNCHRONIZERS/DRIVERS

PARAMETER MEASUREMENT INFORMATION



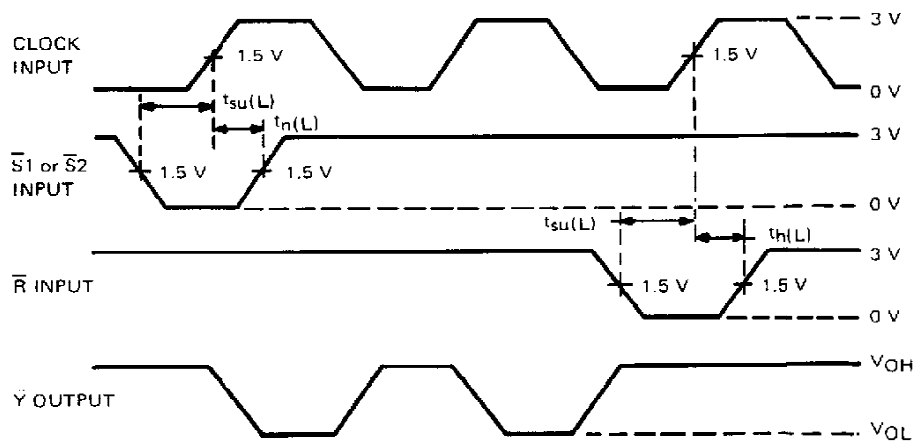
- NOTES: A. The clock input pulse in figures 2 through 5 is supplied by a generator having the following characteristics: $t_w(\text{clock}) \geq 15 \text{ ns}$, $\text{PRR} \leq 1 \text{ MHz}$, and $Z_{out} \approx 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.

FIGURE 1—LOAD CIRCUIT FOR SWITCHING TESTS



NOTE: Mode control and \bar{R} inputs are low and unused \bar{S} input is high.

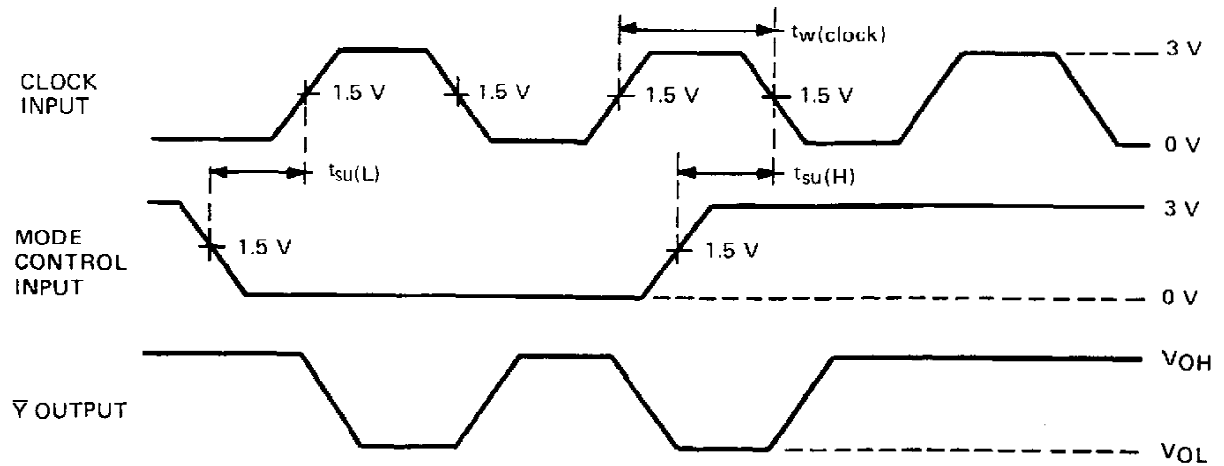
FIGURE 2—INITIATING AND TERMINATING PULSE TRAIN FROM S INPUTS



NOTE: Mode control input is low and unused \bar{S} input is high.

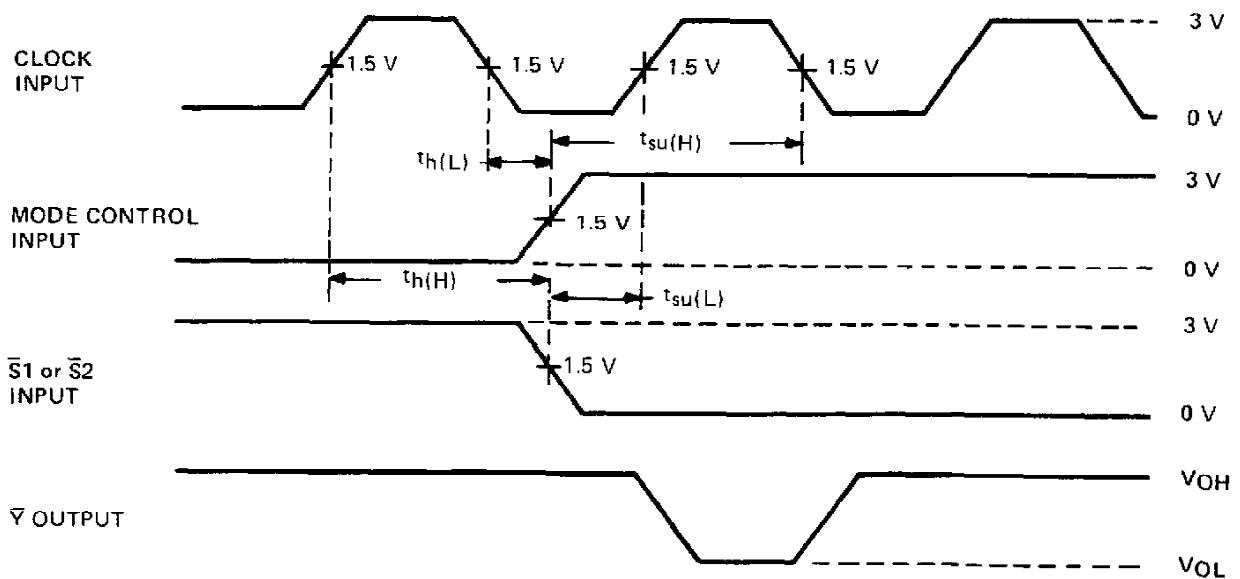
FIGURE 3—INITIATING PULSE TRAIN FROM S AND TERMINATING WITH R INPUTS

PARAMETER MEASUREMENT INFORMATION



NOTE: At least one of the \bar{S} inputs is low.

FIGURE 4—INITIATING AND TERMINATING PULSE TRAIN WITH MODE CONTROL INPUT



NOTE: Input \bar{R} is low and the unused \bar{S} input is high.

FIGURE 5—ENABLING SINGLE PULSE

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.