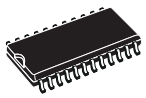
HCF4034B

8 STAGE STATIC BIDIRECTIONAL PARALLEL/SERIAL INPUT OUTPUT BUS REGISTER

- BIDIRECTIONAL PARALLEL DATA INPUT
- PARALLEL OR SERIAL INPUTS/PARALLEL OUTPUTS
- ASYNCHRONOUS OR SYNCHRONOUS PARALLEL DATA LOADING.
- PARALLEL DATA-INPUTS ENABLED ON "A" DATA LINES (3-STATE OUTPUT)
- DATA RECIRCULATION FOR REGISTER EXPANSION
- MULTIPACKAGE REGISTER EXPANSION
- FULLY STATIC OPERATIONAL : DC to 5MHz (Typ.) at V_{DD} = 10V
- QUIESCENT CURRENT SPECIF. UP TO 20V
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



SOP

ORDER CODES

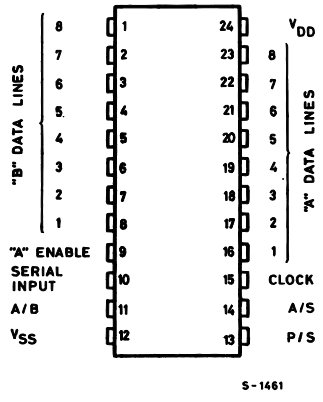
PACKAGE	TUBE	T & R
SOP	HCF4034BM1	HCF4034M013TR

DESCRIPTION

HCF4034B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in SOP packages.

HCF4034B is a static eight-stage parallel-or serial-input parallel-output register. It can be used to : 1) bidirectionally transfer parallel information between two buses ; 2) convert serial data to parallel form and direct the parallel data to either of the two buses ; 3) store (recirculate) parallel data, or 4) accept parallel data from either of the two buses and convert the data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/ SERIAL (P/S). Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided. All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow

PIN CONNECTION

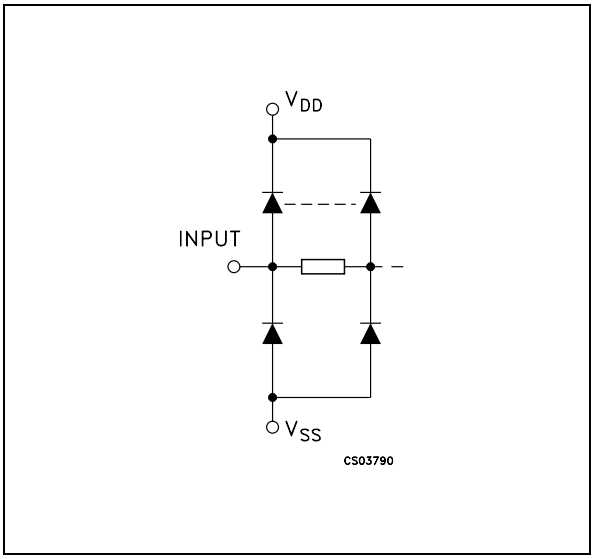


synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION - A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock, provided the A/S input is low. If the A/S input is high, the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs) ; a low A/B signal reverses the direction of data flow. The AE-input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high. Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

SERIAL OPERATION - A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed). The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high). Register expansion can be accomplished by simply cascading HCC/ HCF4034B packages.

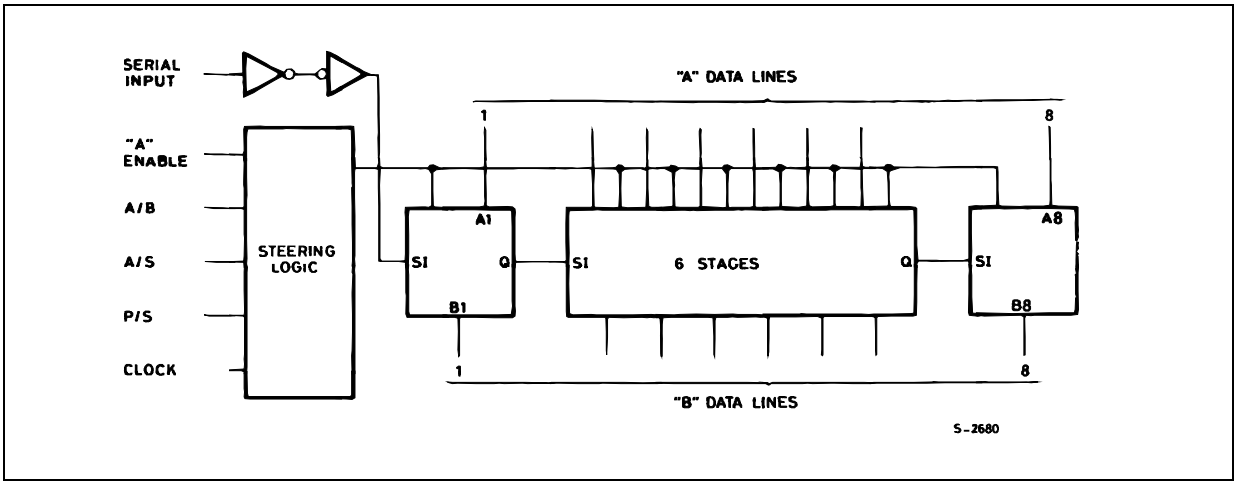
IINPUT EQUIVALENT CIRCUIT



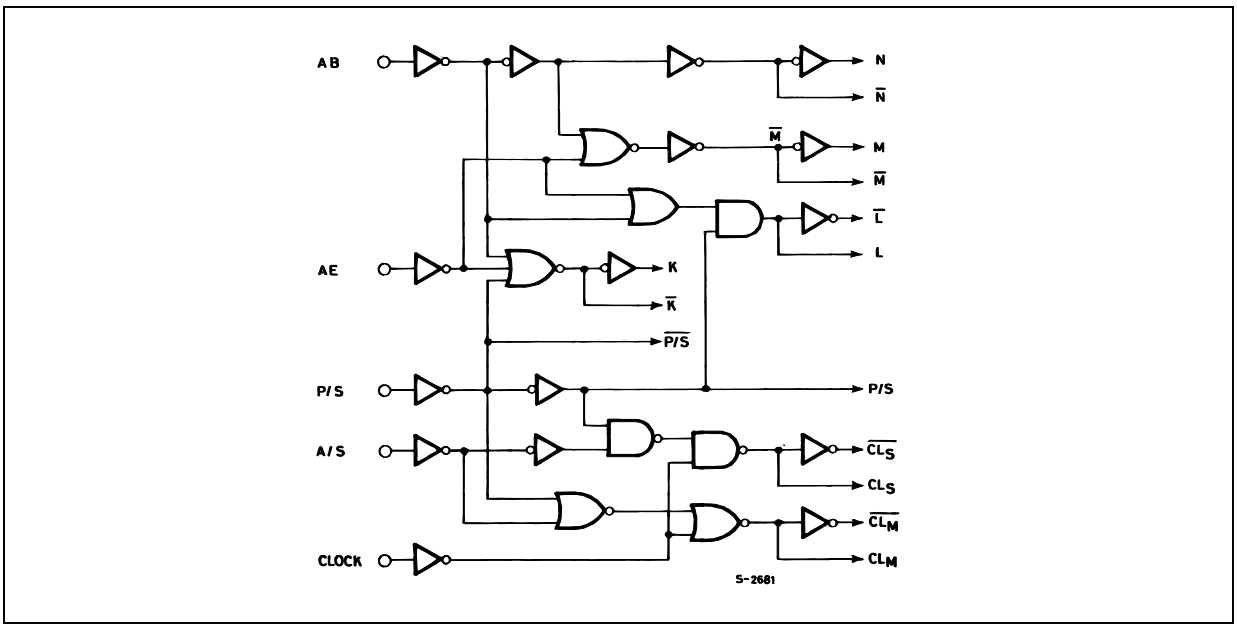
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	1 to 8	B Data Lines
16, 17, 18, 19, 20, 21, 22, 23	1 to 8	A Data Lines
9	AE	"A" Data Enable
15	CL	Clock Input
10	SERIAL INPUT	Serial Data input
11	A/B	"A" Bus to "B" Bus or "B" Bus to "A" Bus Selector
13	P/S	Parallel/Serial Selector
14	A/S	Asynchronous/Synchro-nous Selector
12	V_{SS}	Negative Supply Voltage
24	V_{DD}	Positive Supply Voltage

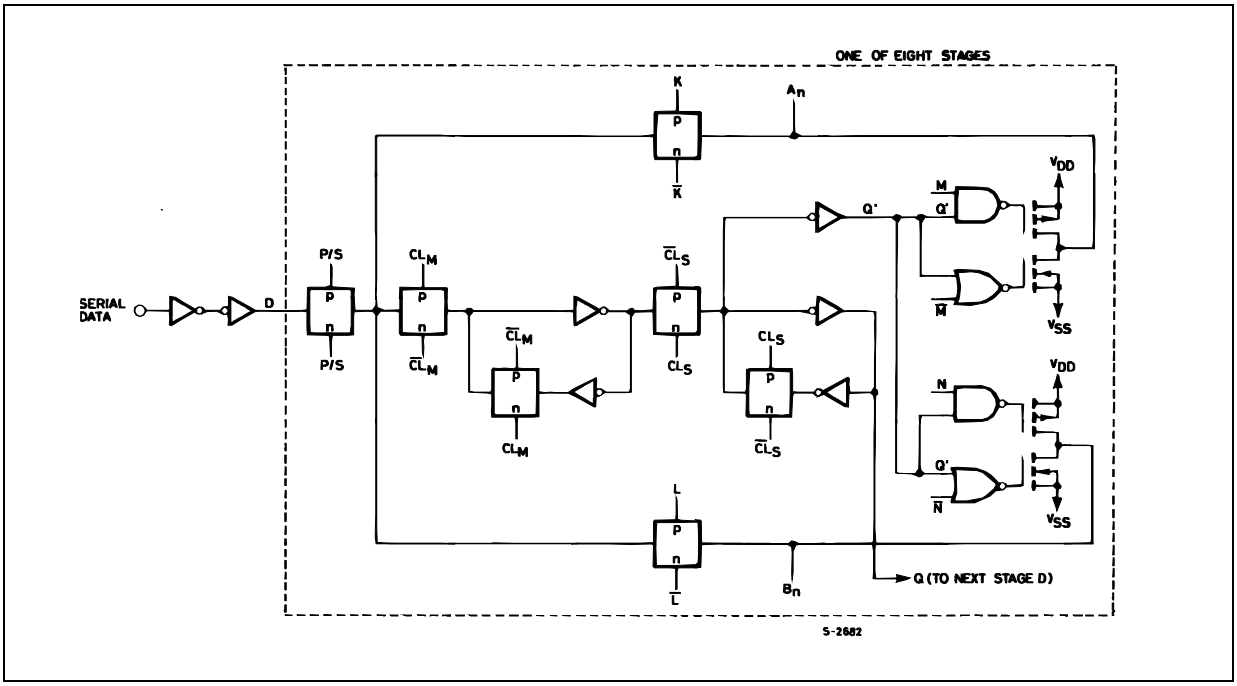
FUNCTIONAL DIAGRAM



LOGIC DIAGRAM (Steering Logic)



LOGIC DIAGRAM (Register Stage 1 Of 8 Stages)



TRUTH TABLE (of the register stage)

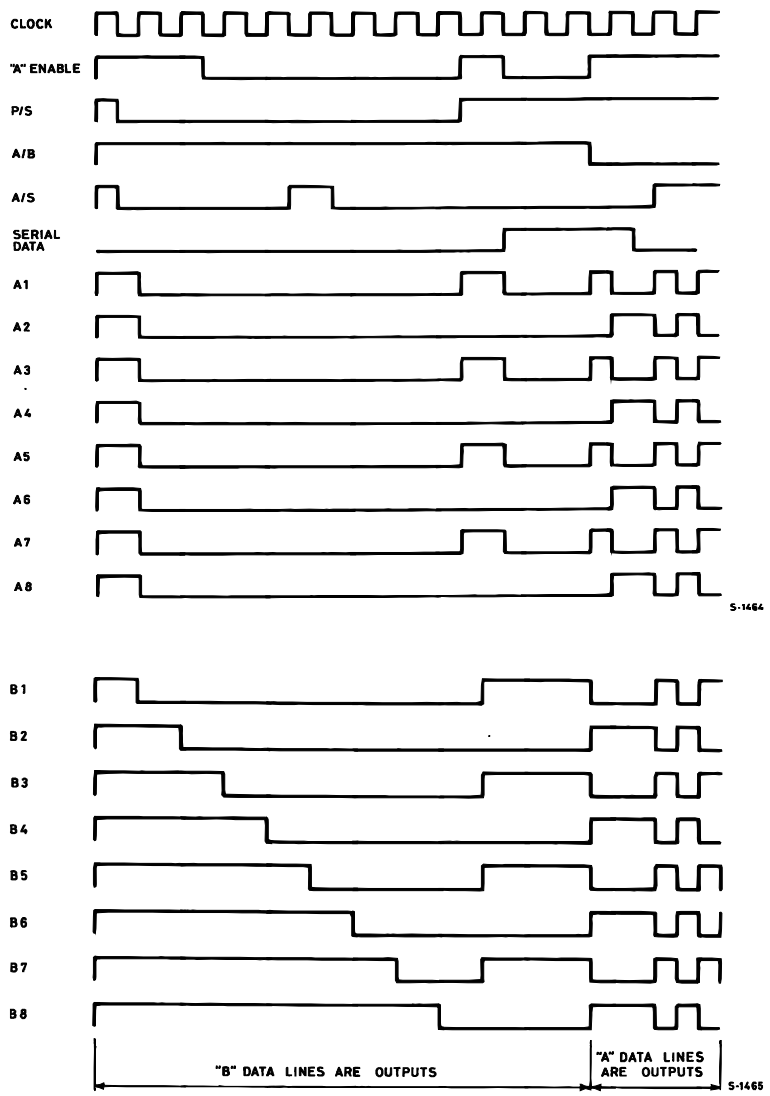
INPUTS			OUTPUT
$\overline{CL}_M$ *	$\overline{CL}_S$ *	D	Q
⌐└	⌐└	L	L
┘⌐	┘⌐	L	L
⌐└	⌐└	L	•
┘⌐	┘⌐	X	L
⌐└	⌐└	H	H
┘⌐	┘⌐	H	H
⌐└	⌐└	H	•

X : Don't Care
* : Level Change
• : Invalid Condition

TRUTH TABLE FOR REGISTER INPUT-LEVELS AND RESULTING REGISTER OPERATION

"A" Enable	P/S	A/B	A/S	OPERATION*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Input Disabled, "B" Parallel Data Output, Synch. Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Input Disabled, "B" Parallel Data Output, Asynch. Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
I_{OZ}	3-State Output Leakage Current	0/18	Any Input		18		$\pm 10^{-4}$	±0.4		±12		±12	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

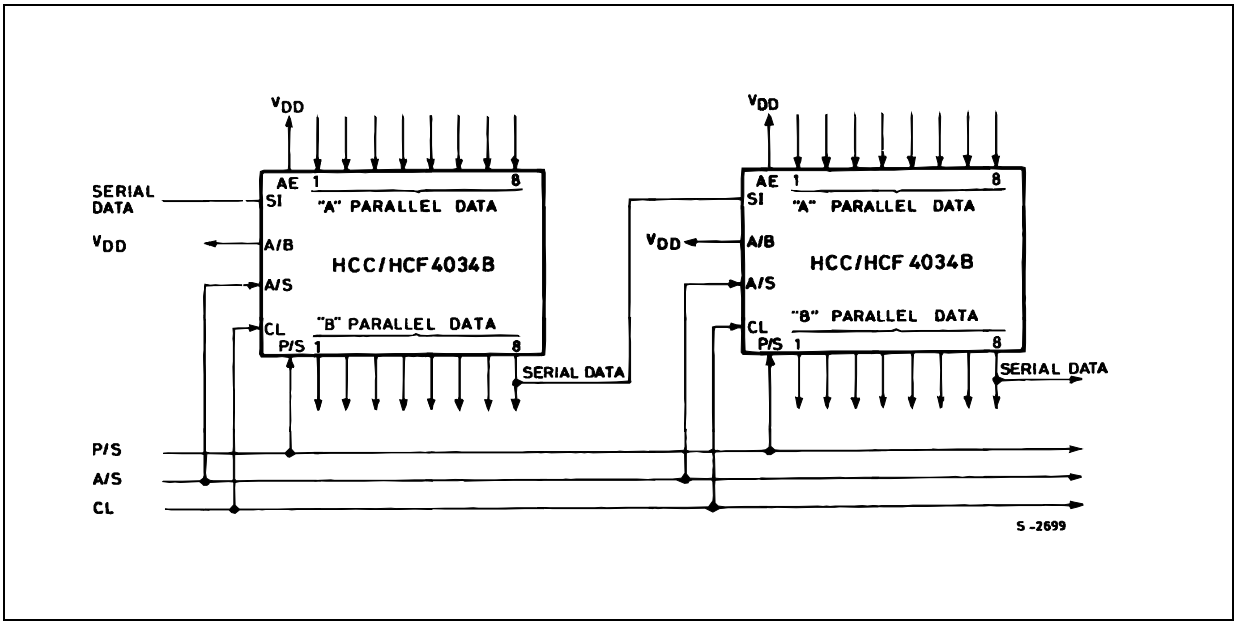
Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time A (B) Parallel Data In to B (A) Parallel Data Out	5			350	700	ns
		10			120	240	
		15			85	170	
t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	3-State Propagation Delay Time A/B or AE to "A" OUT	5			200	400	ns
		10			80	160	
		15			60	120	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{setup}	Data Set-Up Time Serial Data to Clock	5			80	160	ns
		10			30	60	
		15			20	40	
t_{setup}	Data Set-Up Time Parallel Data to Clock	5			25	50	ns
		10			15	30	
		15			10	20	
t_W	High-level Pulse Width, AE, P/S, A/S	5			175	350	ns
		10			70	140	
		15			40	80	
f_{CL}	Maximum Clock Frequency	5		2	4		MHz
		10		5	10		
		15		7	14		
t_W	Clock Pulse Width	5			125	250	ns
		10			50	100	
		15			35	70	
t_r , t_f (1)	Clock Input Rise or Fall Time	5				15	µs
		10				15	
		15				15	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C

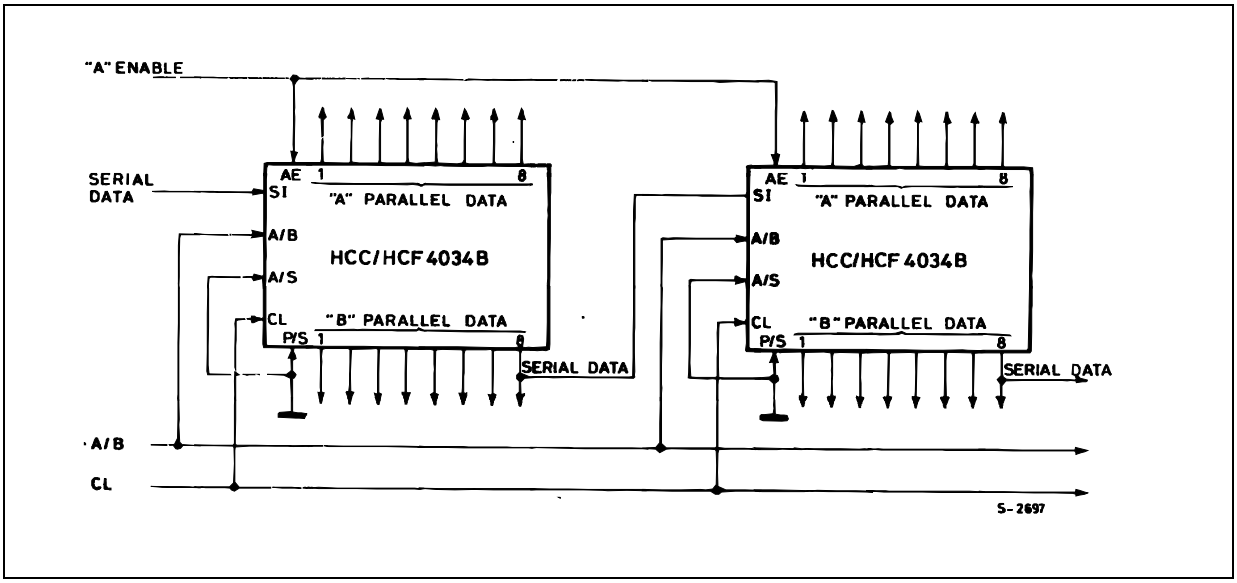
(1) : If more than one unit is cascaded. tr should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TYPICAL APPLICATIONS

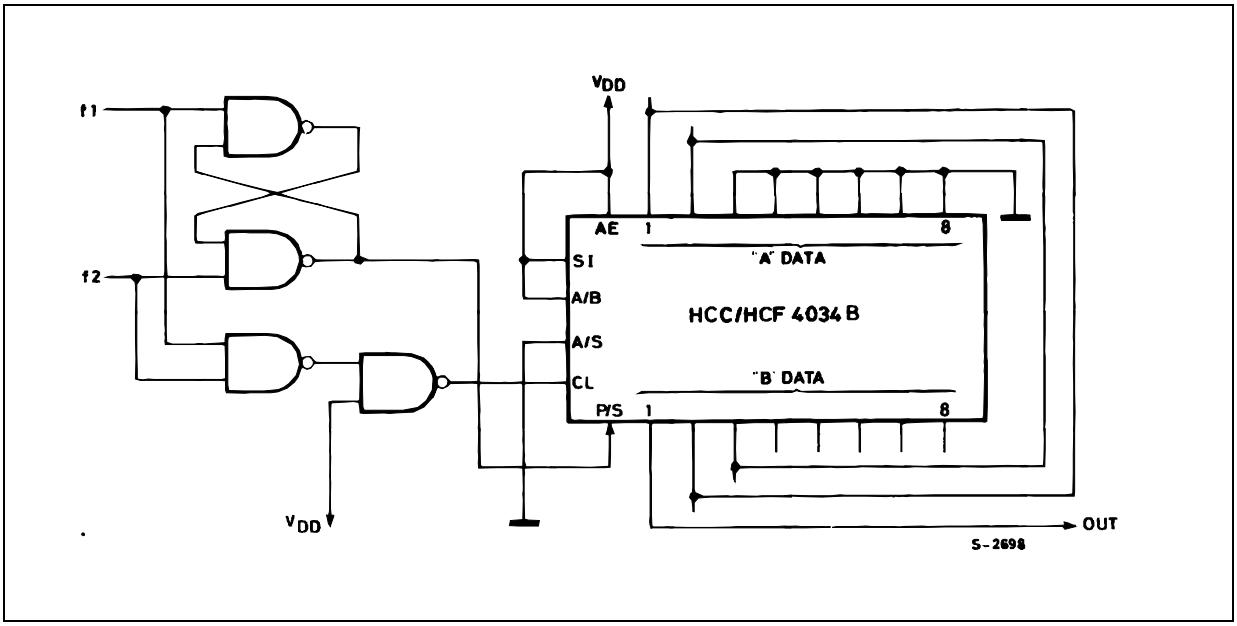
16 BIT PARALLEL IN/PARALLEL OUT PARALLEL IN/SERIAL IN PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER



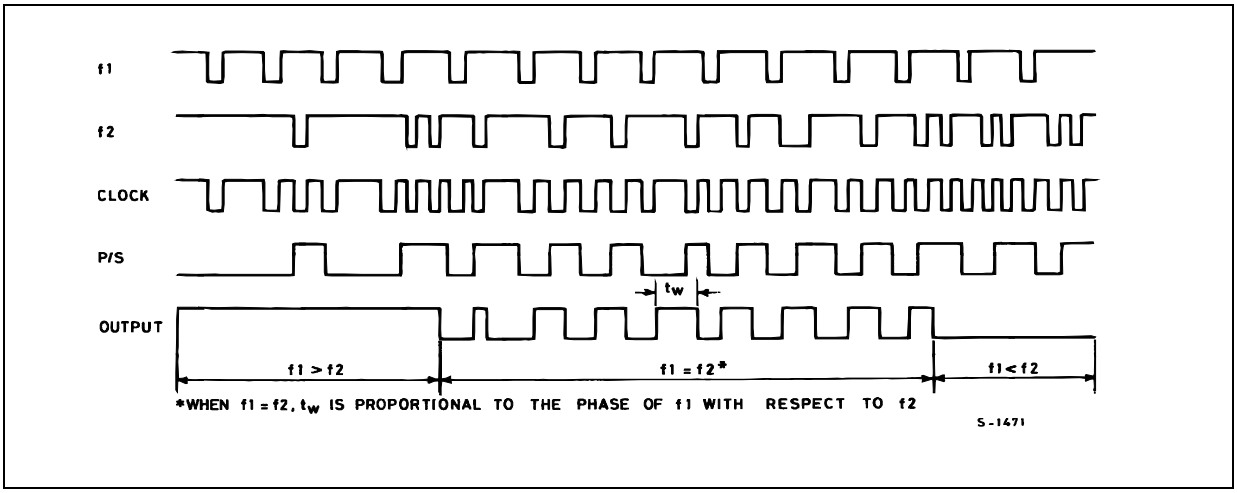
16 BIT SERIAL IN/GATED PARALLEL OUT REGISTER



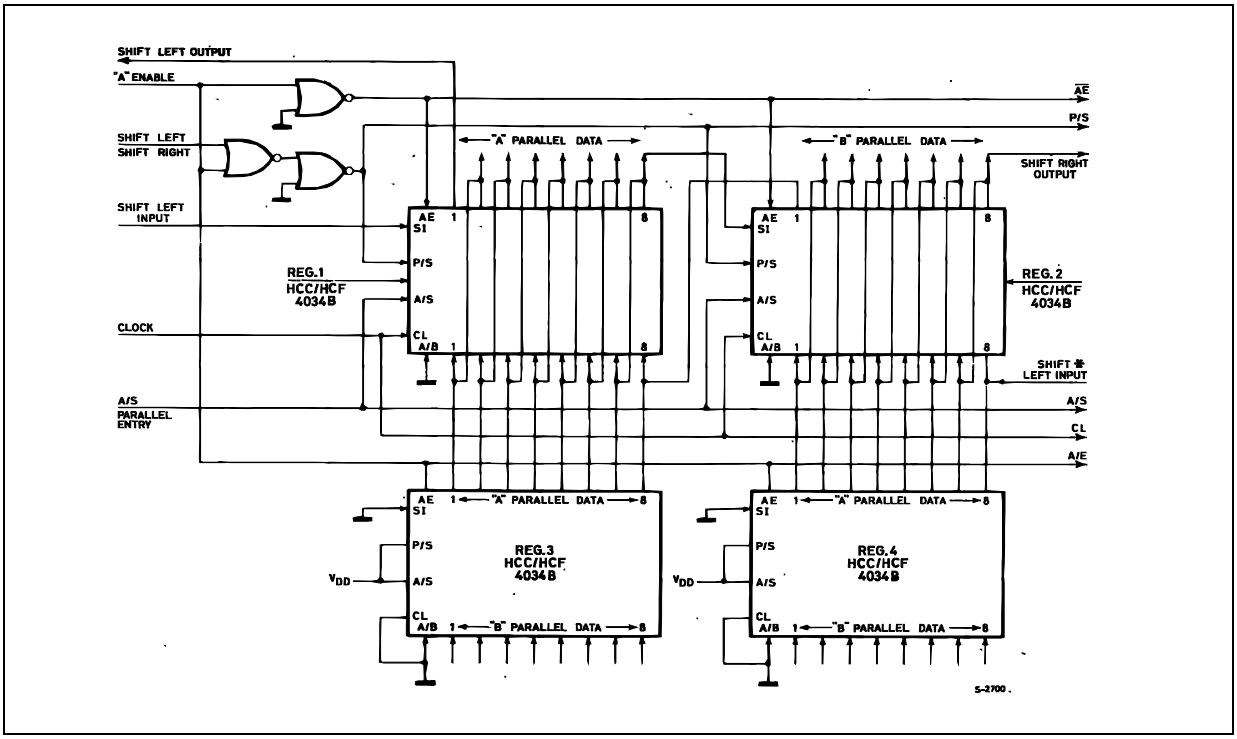
FREQUENCY AND PHASE COMPARATOR



TIMING DIAGRAM



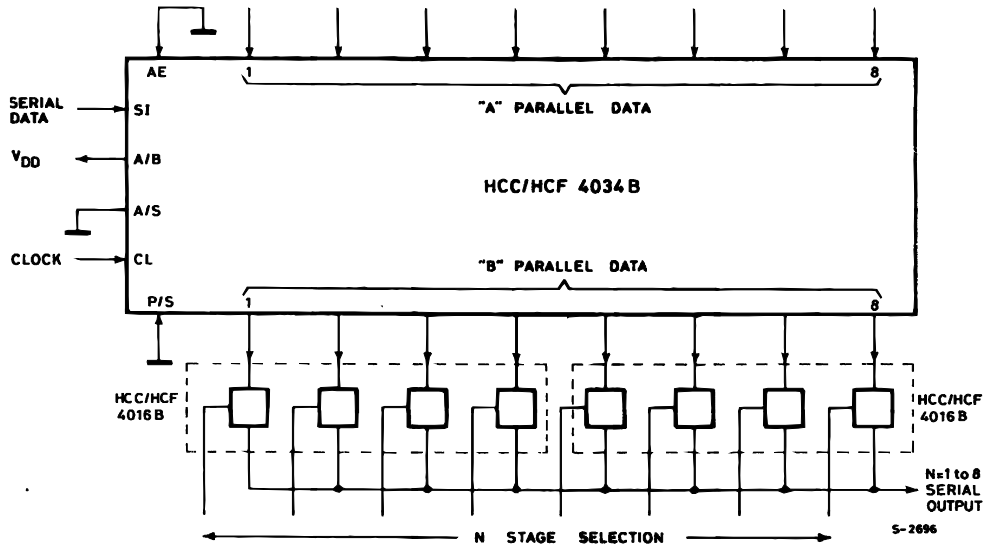
SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



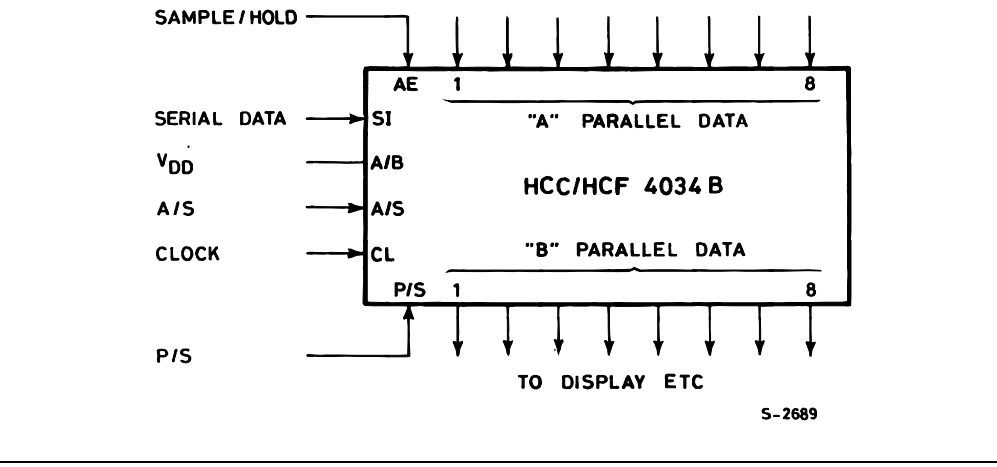
A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logics schemes may be used in place of registers 3 and 4 for parallel loading. When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

* Shift Left input must be disabled during parallel entry.

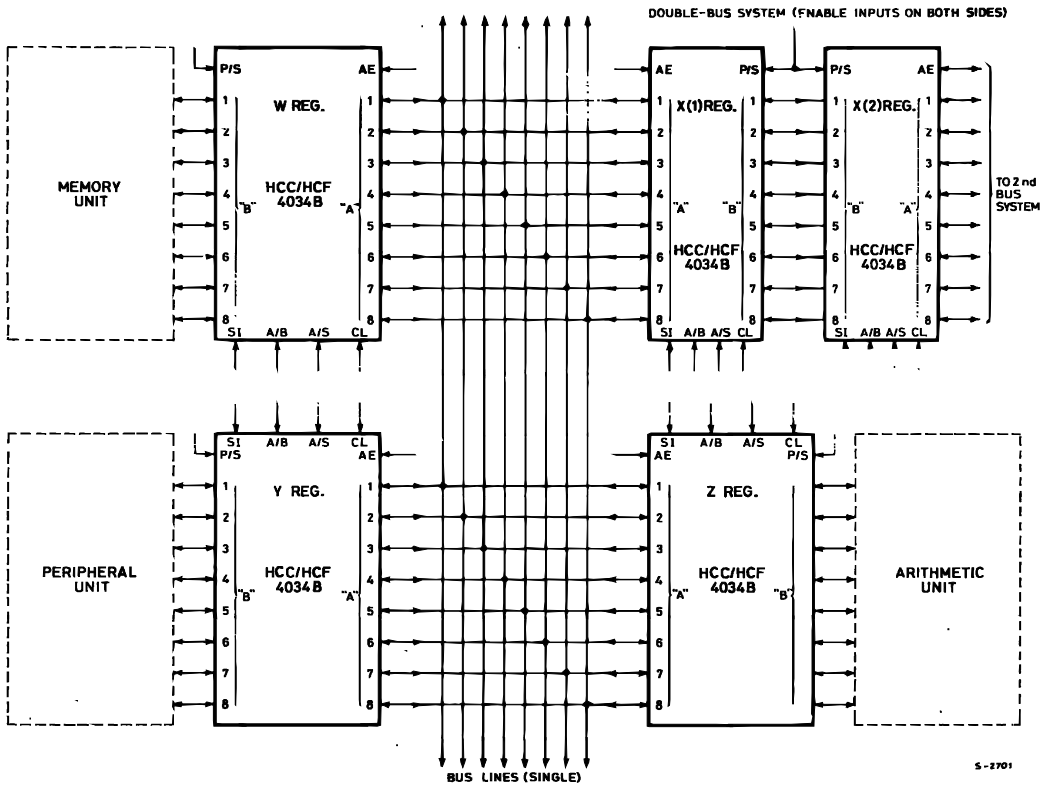
N-STAGE REGISTER WITH FIXED SERIAL OUTPUT LINE



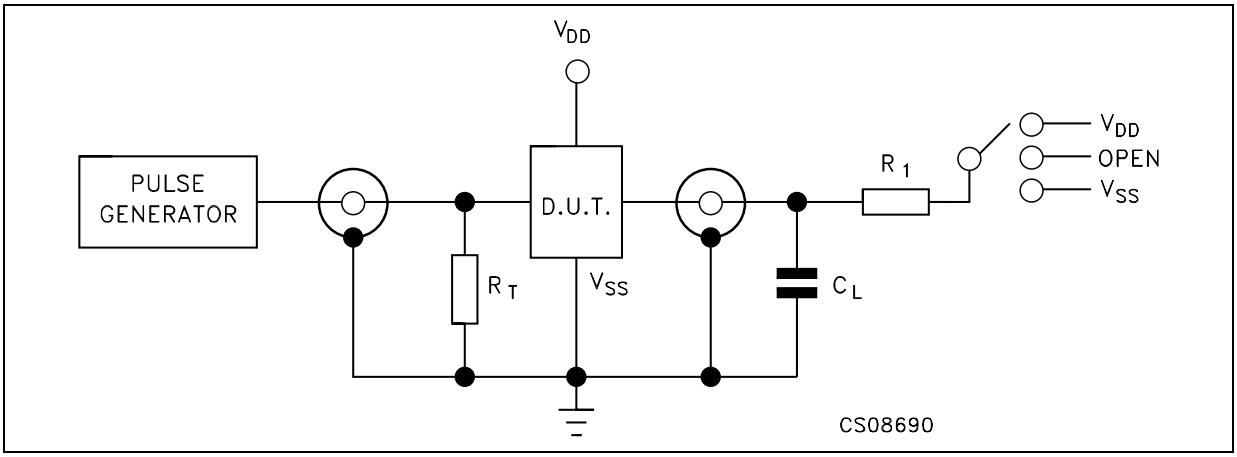
SAMPLE AND HOLD REGISTER-SERIAL/PARALLEL IN-PARALLEL OUT



SINGLE AND DOUBLE BUS SYSTEMS



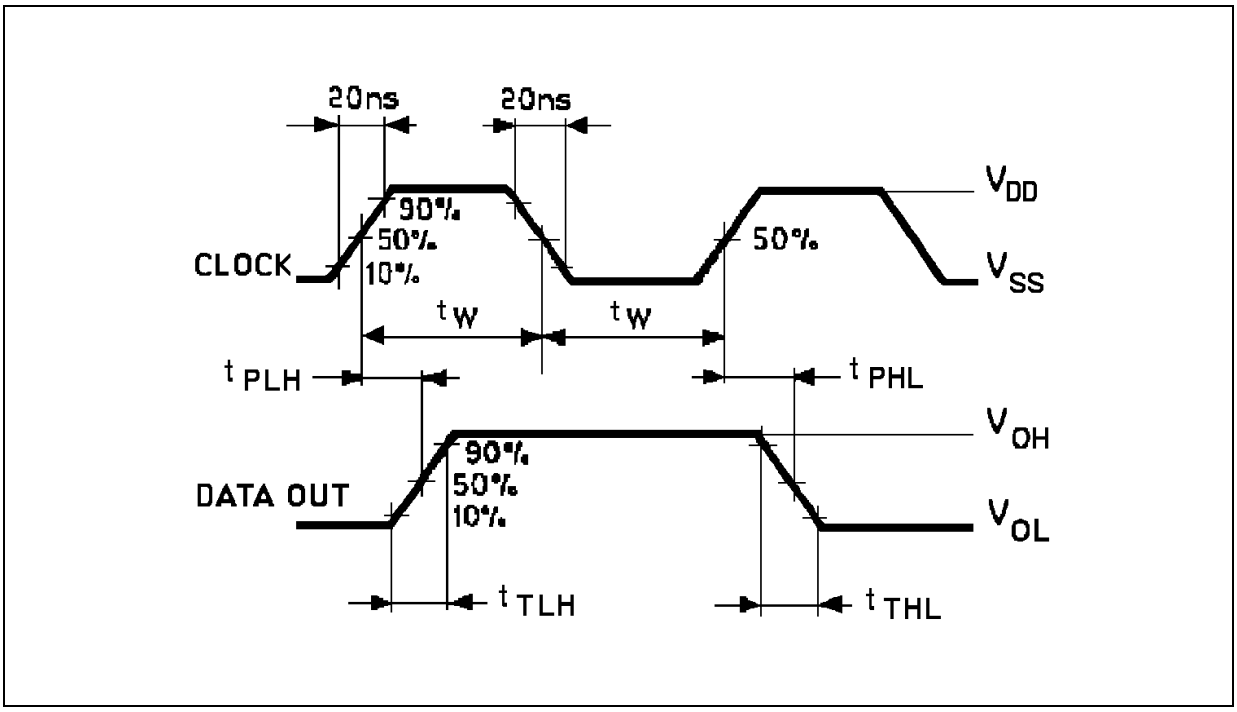
TEST CIRCUIT



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{DD}
t_{PZH}, t_{PHZ}	V_{SS}

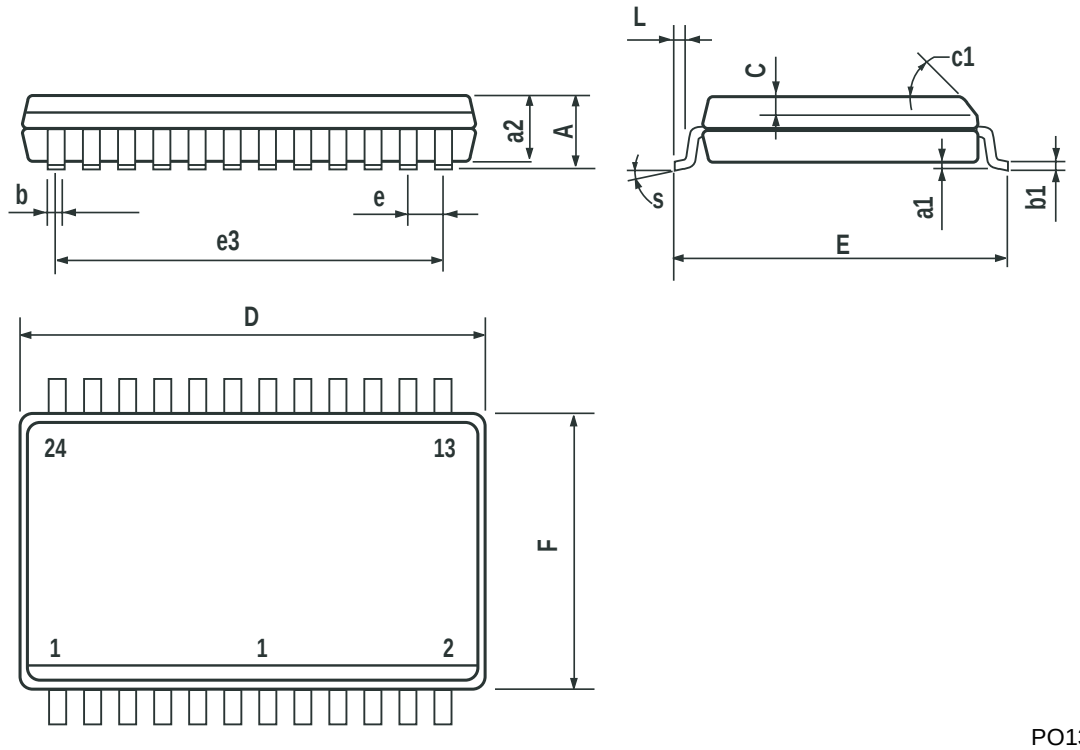
C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



SO-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					



PO13T