

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4015B

MSI

Dual 4-bit static shift register

Product specification
File under Integrated Circuits, IC04

January 1995

Dual 4-bit static shift register

HEF4015B MSI

DESCRIPTION

The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs (O₀ to O₃) and an overriding asynchronous master reset input (MR). Information

present on D is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. A HIGH on MR clears the register and forces O₀ to O₃ to LOW, independent of CP and D. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

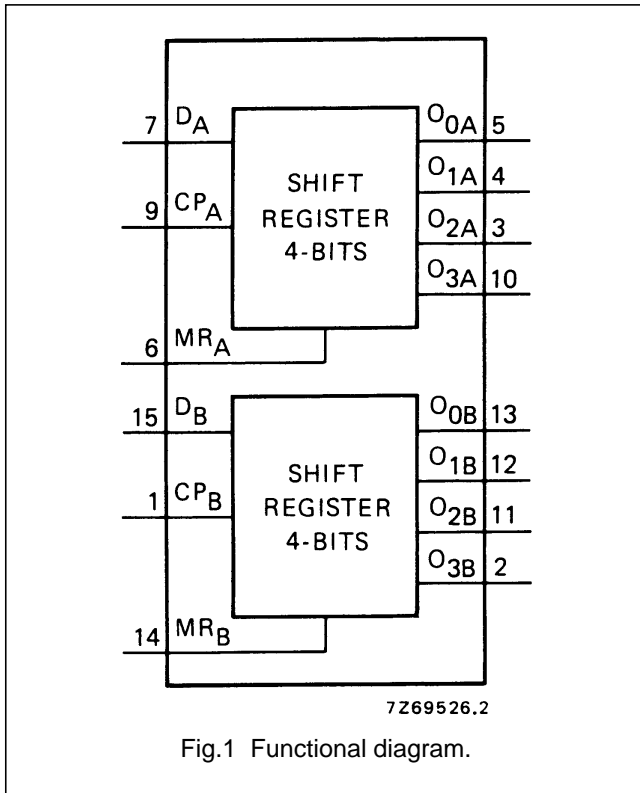


Fig.1 Functional diagram.

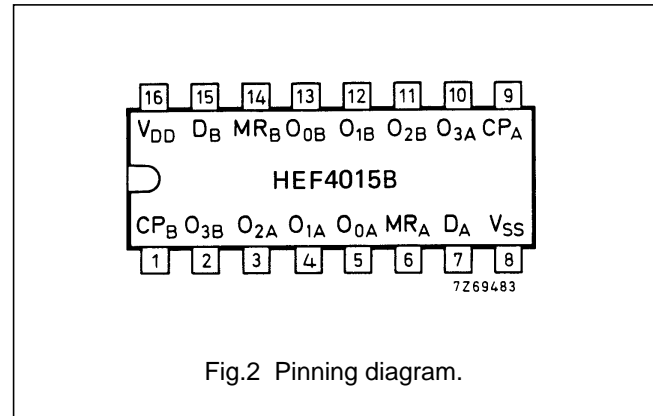


Fig.2 Pinning diagram.

- HEF4015BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4015BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4015BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- D_A, D_B serial data input
- MR_A, MR_B master reset input (active HIGH)
- CP_A, CP_B clock input (LOW-to-HIGH edge-triggered)
- O_{0A}, O_{1A}, O_{2A}, O_{3A} parallel outputs
- O_{0B}, O_{1B}, O_{2B}, O_{3B} parallel outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4015B are:

- Serial-to-parallel converter
- Buffer stores
- General purpose register

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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LOGIC DIAGRAM (one register)

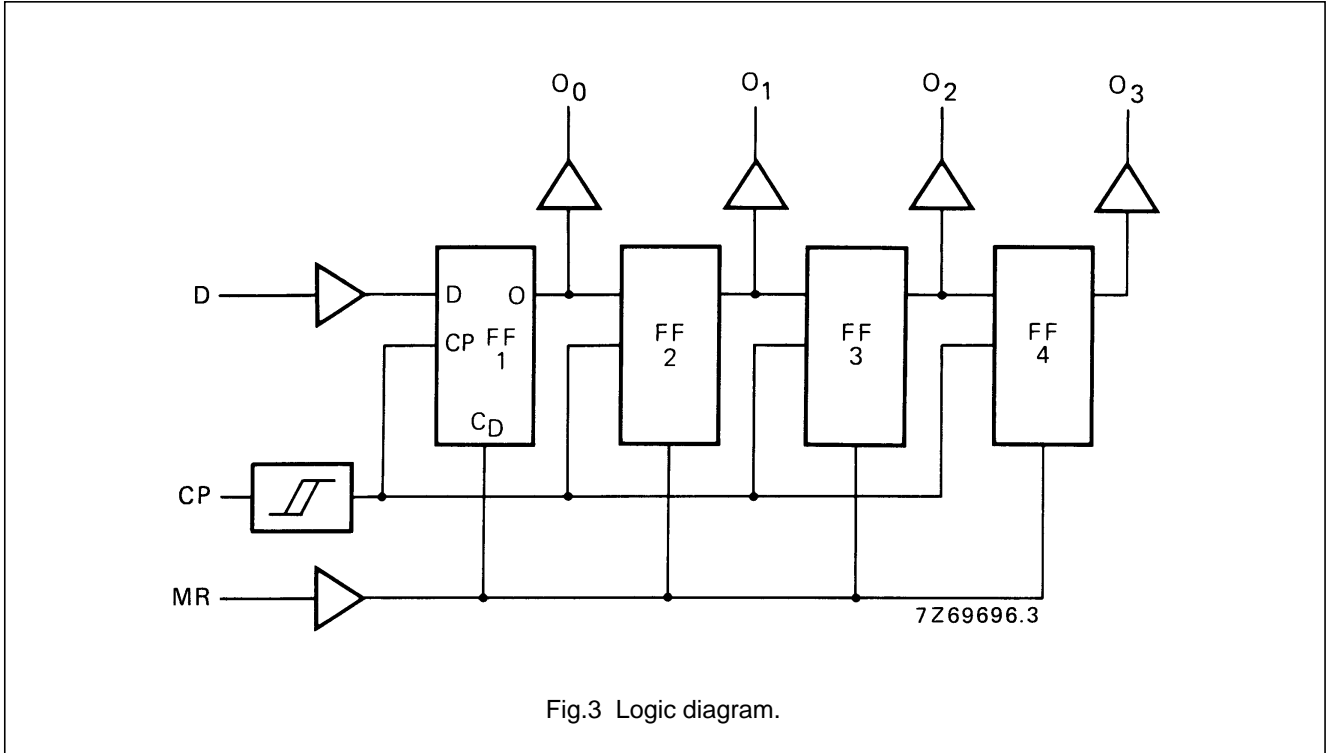


Fig.3 Logic diagram.

FUNCTION TABLE

n	INPUTS			OUTPUTS			
	CP	D	MR	O ₀	O ₁	O ₂	O ₃
1		D ₁	L	D ₁	X	X	X
2		D ₂	L	D ₂	D ₁	X	X
3		D ₃	L	D ₃	D ₂	D ₁	X
4		D ₄	L	D ₄	D ₃	D ₂	D ₁
		X	L	no change			
	X	X	H	L	L	L	L

Note

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. = positive-going transition
5. = negative-going transition
6. D_n = either HIGH or LOW
7. n = number of clock pulse transitions

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays CP \rightarrow O _n HIGH to LOW	5	t_{PHL}		130	260	ns	103 ns + (0,55 ns/pF) C _L
	10			55	110	ns	44 ns + (0,23 ns/pF) C _L
	15			40	80	ns	32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t_{PLH}		120	240	ns	93 ns + (0,55 ns/pF) C _L
	10			55	110	ns	44 ns + (0,23 ns/pF) C _L
	15			40	80	ns	32 ns + (0,16 ns/pF) C _L
MR \rightarrow O _n HIGH to LOW	5	t_{PHL}		105	210	ns	78 ns + (0,55 ns/pF) C _L
	10			45	90	ns	34 ns + (0,23 ns/pF) C _L
	15			35	70	ns	27 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10			30	60	ns	9 ns + (0,42 ns/pF) C _L
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10			30	60	ns	9 ns + (0,42 ns/pF) C _L
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L
Set-up time D \rightarrow CP	5	t_{su}	25	-15		ns	see waveforms Figs 4 and 5
	10		25	-10		ns	
	15		20	-5		ns	
Hold time D \rightarrow CP	5	t_{hold}	40	20		ns	
	10		20	10		ns	
	15		15	8		ns	
Minimum clock pulse width; LOW	5	t_{WCPL}	60	30		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	80	40		ns	
	10		30	15		ns	
	15		24	12		ns	
Recovery time for MR	5	t_{RMR}	50	20		ns	
	10		30	10		ns	
	15		20	5		ns	
Maximum clock pulse frequency	5	f_{max}	7	15		MHz	
	10		15	30		MHz	
	15		22	44		MHz	

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	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5	$1\,500 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6\,300 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$17\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

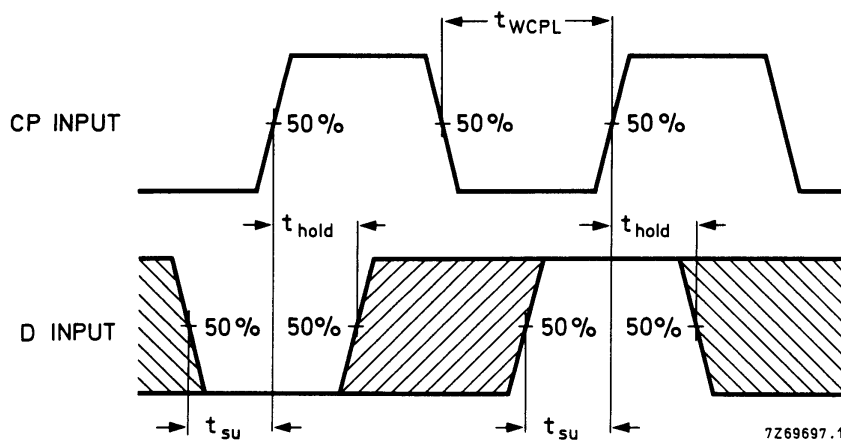


Fig.4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

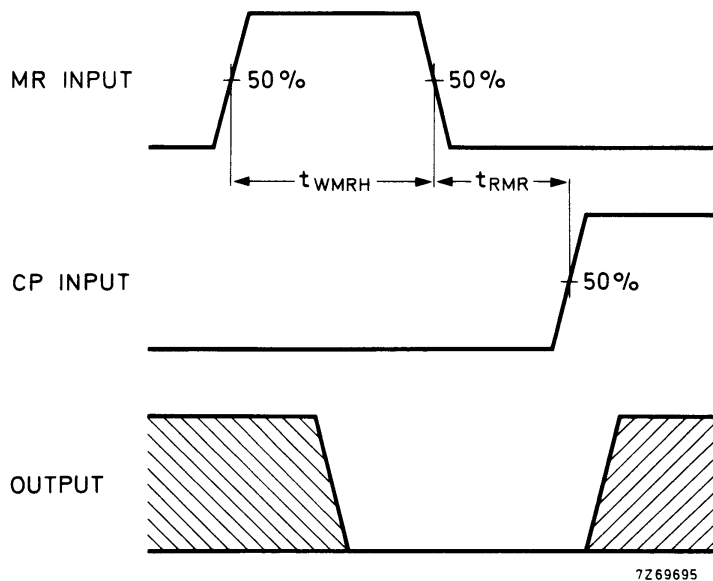


Fig.5 Waveforms showing recovery time for MR and minimum MR pulse width.