MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

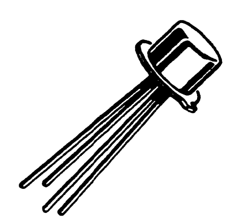
3N128

SILICON N-CHANNEL MOS FIELD-EFFECT TRANSISTOR

. . . designed for VHF amplifier and oscillator applications in communications equipment.

- High Forward Transadmittance — $|y_{fs}|$ = 5000 µmhos (Min) @ f = 1.0 kHz
- Low Input Capacitance — C_{iss} = 7.0 pF (Max) @ f = 1.0 MHz
- Low Noise Figure — NF = 5.0 dB (Max) @ f = 200 MHz
- High Power Gain — P_G = 13.5 dB (Min) @ f = 200 MHz
- Complete "y" Parameter Curves
- Third Order Intermodulation Distortion Performance Curve Provided

N-CHANNEL MOS FIELD-EFFECT TRANSISTOR



* MAXIMUM RATINGS

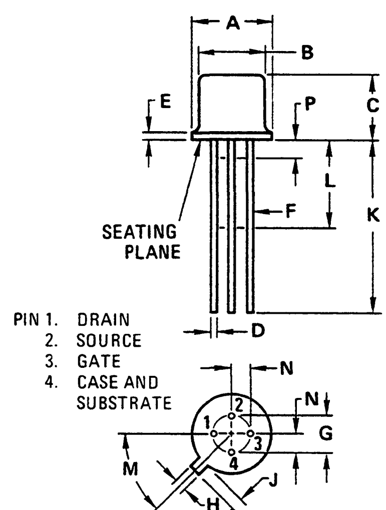
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	+20	Vdc
Drain-Gate Voltage	V_{DG}	+20	Vdc
Gate-Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	50	mAdc
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 2.2	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175	°C

*Indicates JEDEC Registered Data.

HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45°BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

**CASE 20-03
TO-206AF
(TO-72)**

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage (1) (I_G = −10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	-50	—	Vdc
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 50 μAdc)	$V_{GS(off)}$	-0.5	-8.0	Vdc
Gate Reverse Current (V_{GS} = -8.0 Vdc, V_{DS} = 0) (V_{GS} = -8.0 Vdc, V_{DS} = 0, T_A = 125°C)	I_{GSS}	— —	0.05 5.0	nAdc
ON CHARACTERISTICS				
Zero-Gate-Voltage Drain Current (2) (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	5.0	25	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transadmittance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 kHz)	$\|y_{fs}\|$	5000	12,000	μmhos
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	$Re(y_{fs})$	5000	—	μmhos
Output Conductance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	$Re(y_{os})$	—	500	μmhos
Input Conductance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	$Re(y_{is})$	—	800	μmhos
Input Capacitance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 MHz)	C_{iss}	—	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 1.0 MHz)	C_{rss}	0.05	0.35	pF
Noise Figure (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	NF	—	5.0	dB
Power Gain (V_{DS} = 15 Vdc, I_D = 5.0 mAdc, f = 200 MHz)	P_G	13.5	23	dB

*Indicates JEDEC Registered Data.
(1) Caution Destructive Test, can damage gate oxide beyond operation.
(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

TYPICAL CHARACTERISTICS
(T_A = 25°C)

FIGURE 1 — DRAIN CHARACTERISTICS

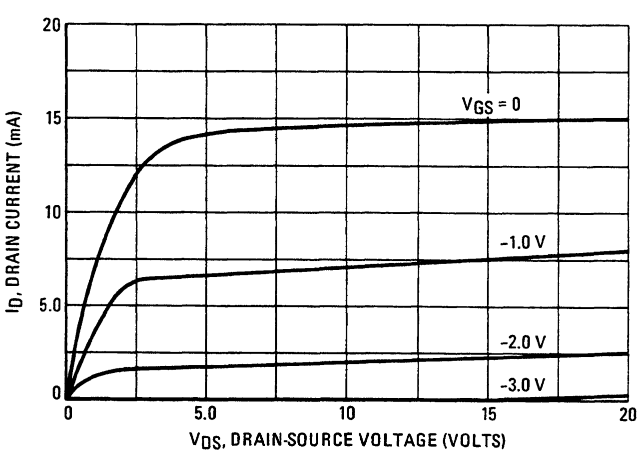
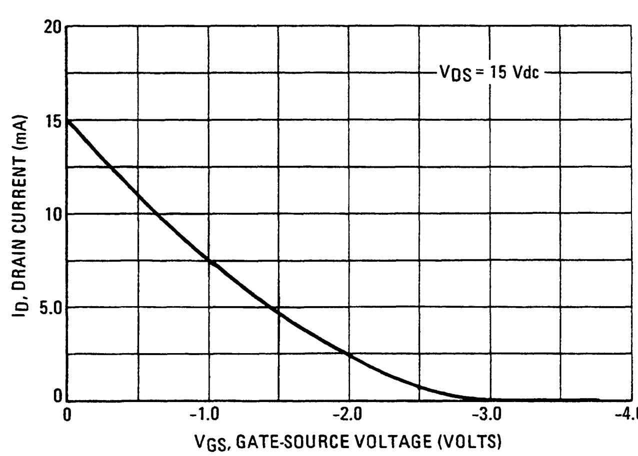


FIGURE 2 — TRANSFER CHARACTERISTICS



TYPICAL 1 kHz DRAIN CHARACTERISTICS

($T_A = 25^oC$, V_{DS} = 15 Vdc, f = 1.0 kHz)

FIGURE 3 – FORWARD TRANSADMITTANCE versus GATE BIAS VOLTAGE

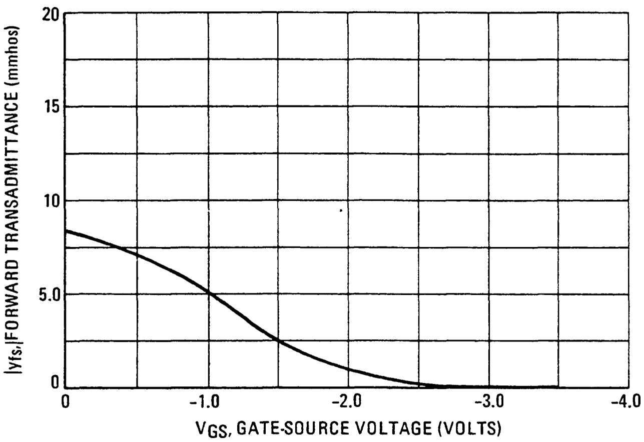
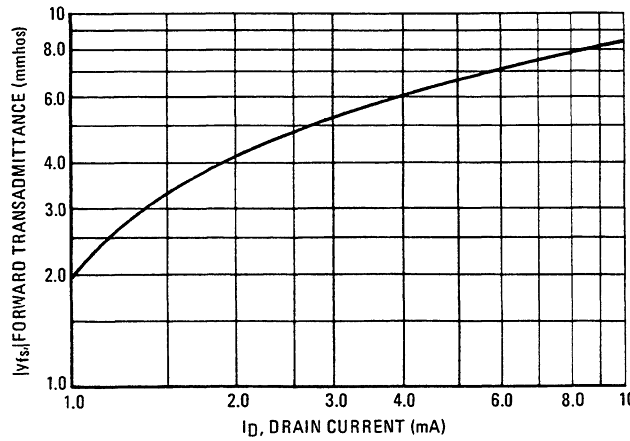


FIGURE 4 – FORWARD TRANSADMITTANCE versus DRAIN CURRENT



TYPICAL 200 MHz COMMON-SOURCE ADMITTANCE CHARACTERISTICS

($T_A = 25^oC$, V_{DS} = 15 Vdc, f = 200 MHz)

FIGURE 5 – INPUT ADMITTANCE (y_{is}) COMPONENTS

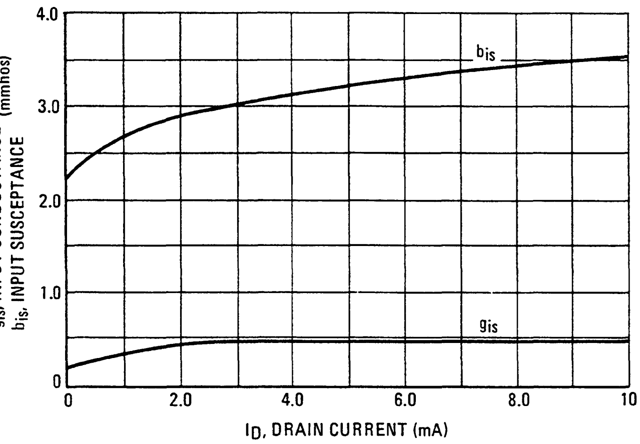


FIGURE 6 – FORWARD TRANSADMITTANCE (y_{fs}) COMPONENTS

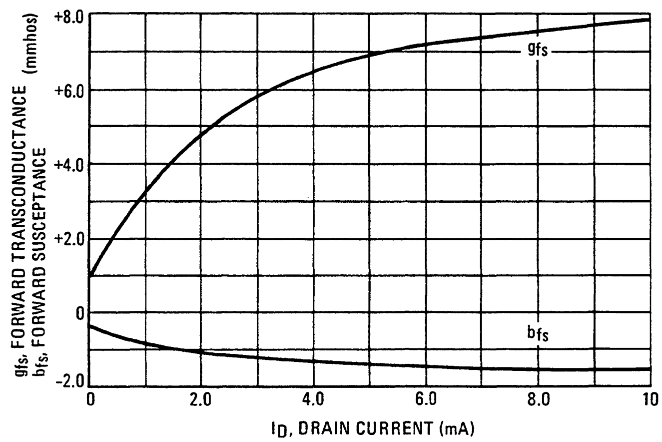


FIGURE 7 – REVERSE TRANSADMITTANCE (y_{rs}) COMPONENTS

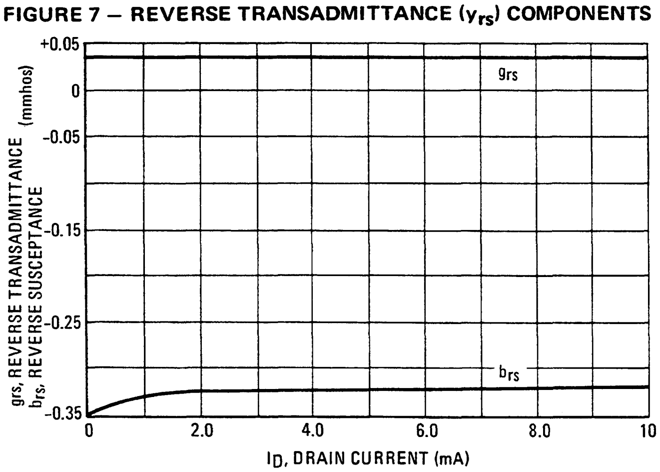


FIGURE 8 – OUTPUT ADMITTANCE (y_{os}) COMPONENTS

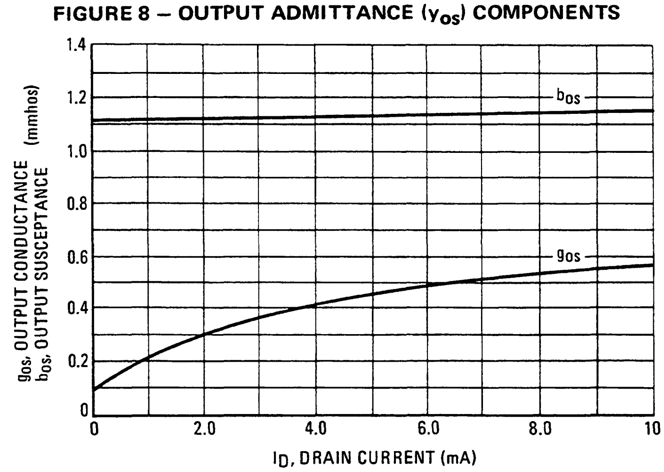


FIGURE 9 — POWER GAIN AND NOISE FIGURE versus DRAIN CURRENT

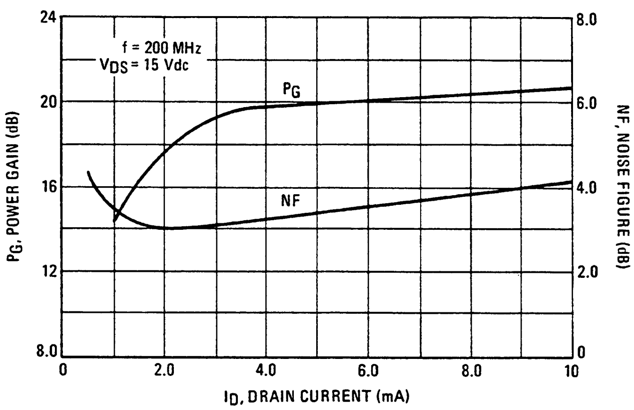


FIGURE 10 — POWER GAIN AND NOISE FIGURE versus DRAIN VOLTAGE

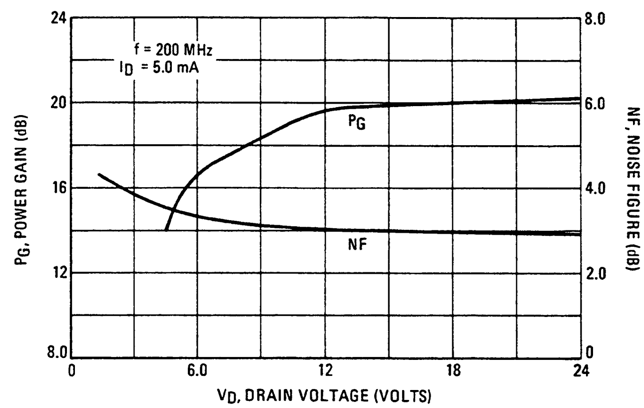


FIGURE 11 — THIRD ORDER INTERMODULATION DISTORTION

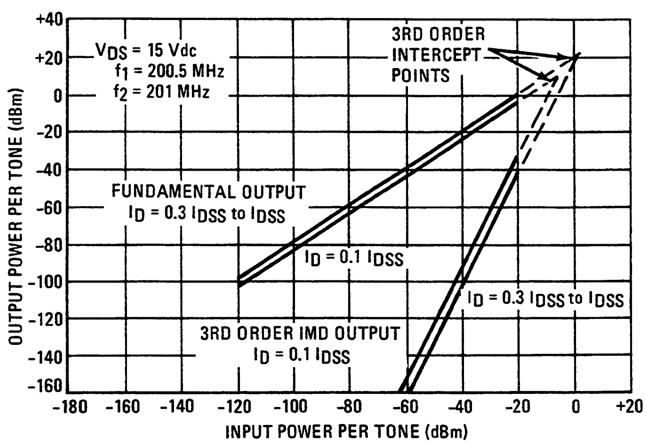
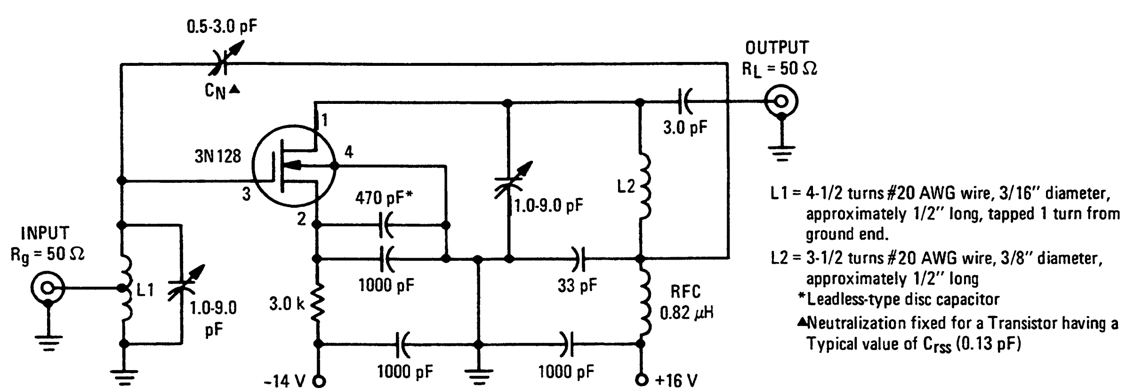


Figure 11 shows the typical third order intermodulation distortion (IMD) performance of the 3N128 at 200 MHz.

Both fundamental output and third order IMD output characteristics are plotted. The curves have been extrapolated to show the third order intermodulation output intercept point.

Performance for drain currents from I_{DSS} to 0.1 I_{DSS}, is given. The power gain and noise figure test amplifier shown in Figure 12 was used to generate the IMD data.

FIGURE 12 — POWER GAIN, NOISE FIGURE AND INTERMODULATION DISTORTION TEST CIRCUIT



L1 = 4-1/2 turns #20 AWG wire, 3/16" diameter, approximately 1/2" long, tapped 1 turn from ground end.
L2 = 3-1/2 turns #20 AWG wire, 3/8" diameter, approximately 1/2" long
*Leadless-type disc capacitor
▲Neutralization fixed for a Transistor having a Typical value of C_{rss} (0.13 pF)

MOTOROLA Semiconductor Products Inc.

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7669-3 PRINTED IN USA (1994) MPS/POD

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