

3875081 G E SOLID STATE
High-Voltage Power Transistors

File Number 321

2N5239, 2N5240

High-Voltage, Silicon N-P-N Transistors

For High-Speed Switching and Linear-Amplifier Applications in Industrial and Commercial Service

Features:

- High voltage ratings: $V_{CE(sus)}$
=350 V, $R_{BE} \leq 50 \Omega$ (2N5240)
=250 V, $R_{BE} \leq 50 \Omega$ (2N5239)
- High power dissipation rating:
 $P_T = 100$ W at $V_{CE} = 125$ V, $T_C = 25^\circ$ C
- For switching applications where circuit values and operating conditions require a transistor with a high second-breakdown rating ($I_{S/B}$) (limit line begins at 125 V)
- Exceptional second-breakdown: 0.8 A at $V_{CE} = 125$ V
- Maximum area-of-operation curves for dc and pulse operation

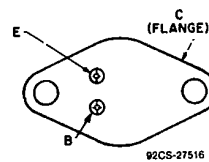
The RCA-2N5239 and 2N5240* are multi epitaxial silicon n-p-n power transistors.

The high breakdown voltage ratings and exceptional second-breakdown capabilities of these transistors make them especially suitable for use in series regulators, power amplifiers, inverters, deflection circuits, switching regulators, and high-voltage bridge amplifiers.

These types differ in breakdown voltage and leakage current values. The 2N5239 and 2N5240 are supplied in steel JEDEC TO-204AA hermetic packages.

* RCA Dev. No. TA2765 and TA2765A, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

MAXIMUM RATINGS, Absolute-Maximum Values:

	2N5239	2N5240	
V_{CEO}	300	375	V
$V_{CE(sus)}$ $R_{BE} \leq 50 \Omega$	250	350	V
$V_{CE(sus)}$	225	300	V
V_{EBO}		6	V
I_C		5	A
I_B		2	A
P_T		100	W
$T_C \leq 25^\circ$ C and $V_{CE} \leq 125$ V		See Fig. 1	
$T_C \leq 25^\circ$ C and $V_{CE} \leq 125$ V		See Fig. 1	
$T_C > 25^\circ$ C and $V_{CE} > 125$ V		-65 to 200	$^\circ$ C
$T_{\theta J}, T_J$			
T_L At distance $\geq 1/32$ in. (0.8 mm) from seating plane for 10 s max.		230	$^\circ$ C

* In accordance with JEDEC registration data

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ELECTRICAL CHARACTERISTICS, At Case Temperature (T_c) = 25°C unless otherwise specified

CHARACTERISTIC	TEST CONDITIONS				LIMITS				UNITS
	VOLTAGE V dc		CURRENT A dc		2N5239		2N5240		
	V _{CE}	V _{BE}	I _c	I _b	Min.	Max.	Min.	Max.	
I _{CEO}	200			0	—	5	—	2	mA
I _{CEV}	300	-1.5			—	4	—	—	
	375	-1.5			—	—	—	2	
($T_c = 150^\circ\text{C}$)	300	-1.5			—	5	—	3	
I _{EBO} (V _{EB} = 5 V) (V _{EB} = 6 V)			0		—	5	—	1	mA
			0		—	20	—	20	
V _{EBO}				0.02	6	—	6	—	V
V _{CEO(sus)} ^a			0.2 ^b		225	—	300	—	
V _{CER(sus)} ^a (R _{BE} ≤ 50 Ω)			0.2 ^b		250	—	350	—	
h _{FE}	10		0.4 ^b		20	80	20	80	
	10		2 ^b		20	80	20	80	
	10		4.5 ^b		5	—	5	—	
V _{BE}	10		2 ^b		—	3	—	3	V
V _{CE(sat)}			2 ^b 4.5 ^b	0.25 1.125	— —	2.5 5	— —	2.5 5	
I _{s/b} (t = 1 s)	125				0.8	—	0.8	—	A
h _{ie} (f = 1 MHz)	10		0.2		2	—	2	—	
h _{ie} (f = 1 kHz)	10		4		20	—	20	—	
f _T	10		0.2		2	—	2	—	MHz
C _{obo} (f = 1 MHz)	10 ^c		0		—	250	—	250	pF
R _{θJC}					—	1.75	—	1.75	°C/W

* In accordance with JEDEC registration data.

^a CAUTION: The sustaining voltages V_{CEO(sus)} and V_{CER(sus)} MUST NOT be measured on a curve tracer.

^b Pulsed; pulse duration ≤ 350 μs, duty factor ≤ 2%.

^c V_{CE} value.

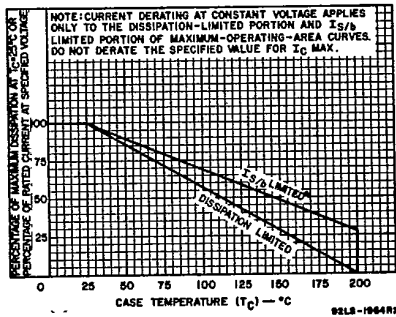


Fig. 1 - Derating curves for both types.

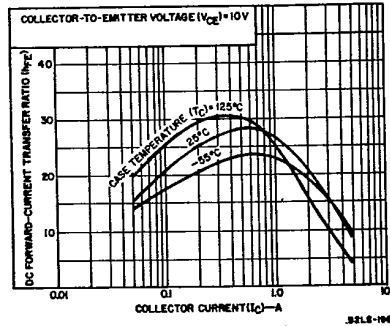


Fig. 2 - Typical dc beta characteristics for both types.

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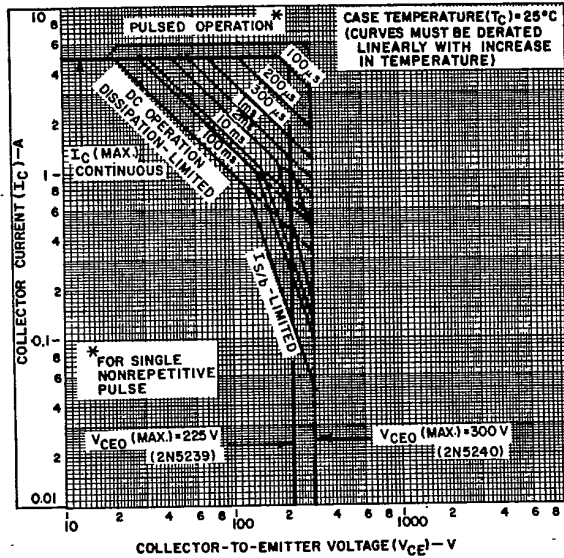


Fig. 3 - Maximum operating areas for both types.

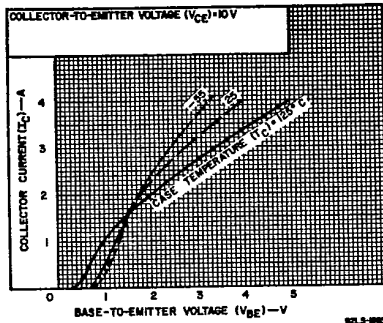


Fig. 4 - Typical transfer characteristics for both types.

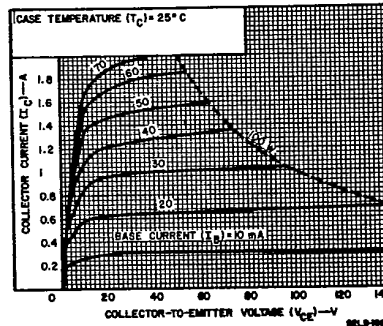


Fig. 5 - Typical output characteristics for both types.

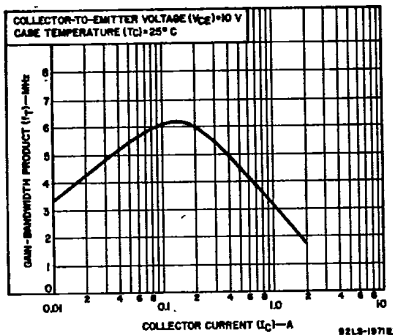


Fig. 6 - Typical gain-bandwidth product as a function of collector current for both types.

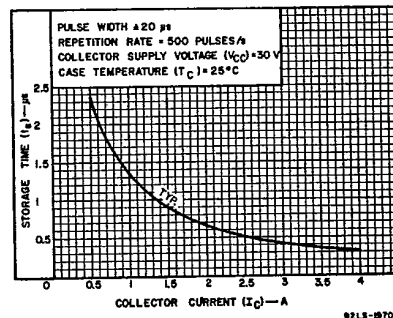


Fig. 7 - Typical saturated-switching time (storage) as a function of collector current for both types.

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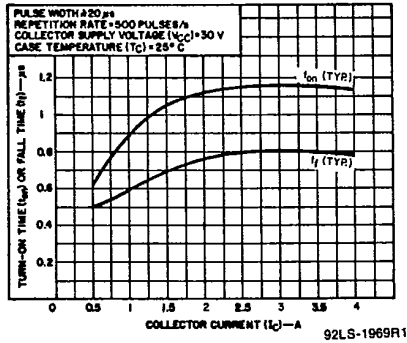


Fig. 8 — Typical saturated-time (turn-on or fall) as a function of collector current for both types.

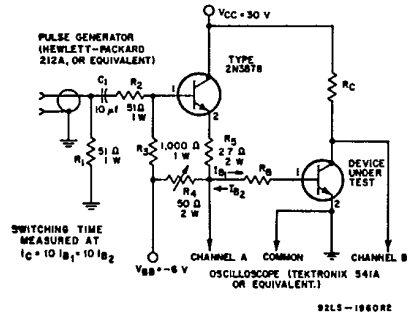


Fig. 9 — Circuit used to measure sustaining voltages, $V_{CE0(sus)}$ and $V_{CEr(sus)}$ for both types.

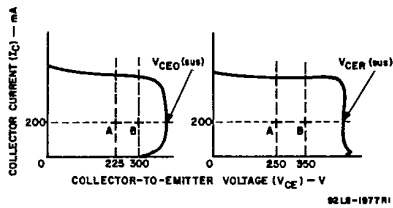


Fig. 10 — Oscilloscope display for $V_{CE0(sus)}$ and $V_{CEr(sus)}$ measurement.

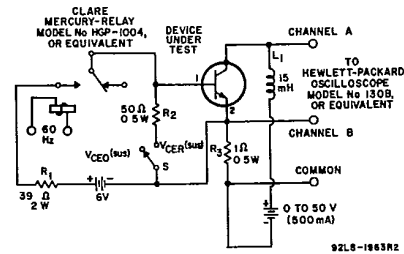


Fig. 11 — Circuit used to measure switching times for both types.

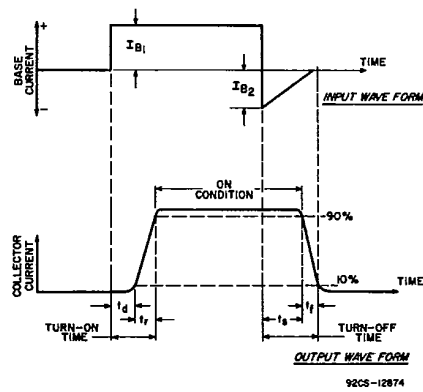


Fig. 12 — Phase relationship between input and output currents showing reference points for specification of switching times.