ECG® Semiconductors

ECG2052

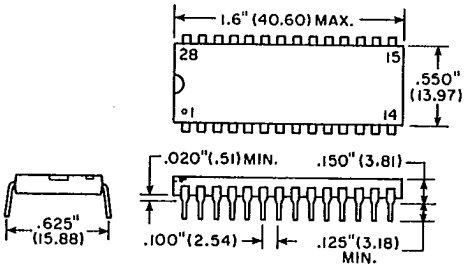
CMOS 3½ Digit DVM with Multiplexed 7-Segment Output

Features

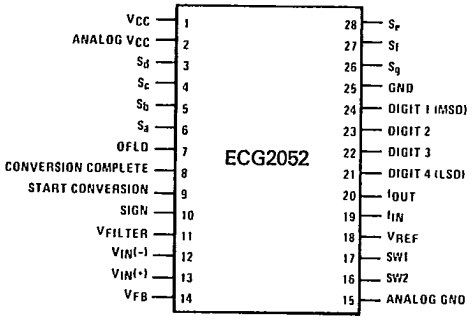
- Operates from single 5 V supply
- Converts 0 V to ±1.999 V
- Multiplexed 7-segment
- No external precision component necessary
- Accuracy specified over temperature
- Medium speed — 200 ms/conversion
- All inputs and outputs TTL compatible
- Internal clock set with RC network or driven externally
- No offset adjust required
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog tranducers (temperature, pressure, displacement, etc.) to digital transducers



Connection Diagram



General Description

The ECG2052 monolithic DVM circuit is manufactured using CMOS technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5 V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ECG2052 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included on this device.

Absolute Maximum Rating (Note 1)

Voltage at Any Pin Except Start Conversion ... -0.3 V to $V_{CC}+0.3$ V
Voltage at Start Conversion ..... -0.3 V to $+15.0$ V
Operating Temperature Range (T_A) ..... $-40°C$ to $+85°C$
Package Dissipation at $T_A=25°C$ ..... 800 mW
Derate at $\theta_{JA(MAX)}=125°C$/Watt above $T_A=25°C$
Operating V_{CC} Range ..... 4.5 V to 6.0 V
Absolute Maximum V_{CC} ..... 6.5 V
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Storage Temperature Range ..... $-65°C$ to $+150°C$

Electrical Characteristics ($4.75\ V \leq V_{CC} \leq 5.25\ V$, $-40°C \leq T_A \leq +85°C$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Units
Logical "1" Input Voltage	$V_{IN(1)}$		V_{CC}-1.5			V
Logical "0" Input Voltage	$V_{IN(0)}$				1.5	V
Logical "0" Output Voltage (All Digital Outputs Except Digit Outputs)	$V_{OUT(0)}$	$I_O=1.6$ mA			0.45	V
Logical "0" Output Voltage (Digit Outputs)	$V_{OUT(0)}$	$I_O=0.9$ mA			0.4	V
Logical "1" Output Voltage (All Segment Outputs)	$V_{OUT(1)}$	$I_O=65$ mA@$T_J=25°C$ $I_O=40$ mA@$T_J=100°C$	V_{CC}-1.6 V_{CC}-1.6	V_{CC}-1.3 V_{CC}-1.3		V V
Logical "1" Output Voltage (All Digital Outputs Except Segment Outputs)	$V_{OUT(1)}$	$I_O=500\mu A$ (Digit Outputs) $I_O=360\mu A$ (Conv. Complete, +/−, Oflo Outputs)	V_{CC}-0.4			V
Output Source Current (Digit Outputs)	I_{SOURCE}	$V_{OUT}=1.0$ V	2.0			mA
Logical "1" Input Current (Start Conversion)	$I_{IN(1)}$	$V_{IN}=1.5$ V			1.0	μA
Logical "0" Input Current (Start Conversion)	$I_{IN(0)}$	$V_{IN}=0$ V	−1.0			μA
Supply Current	I_{CC}	Segments and Digits Open		0.5	10	mA
Oscillator Frequency	f_{osc}			0.6/RC		kHz
Clock Frequency	f_{IN}		100		640	kHz
Conversion Rate	f_C			64,256/f_{IN}		Conv./sec
Digit Mux Rate	f_{MUX}			$f_{IN}/256$		Hz
Inter Digit Blanking Time	t_{BLANK}			1/(32f_{MUX})		sec
Start Conversion Pulse Width	t_{SCPW}		200		DC	ns

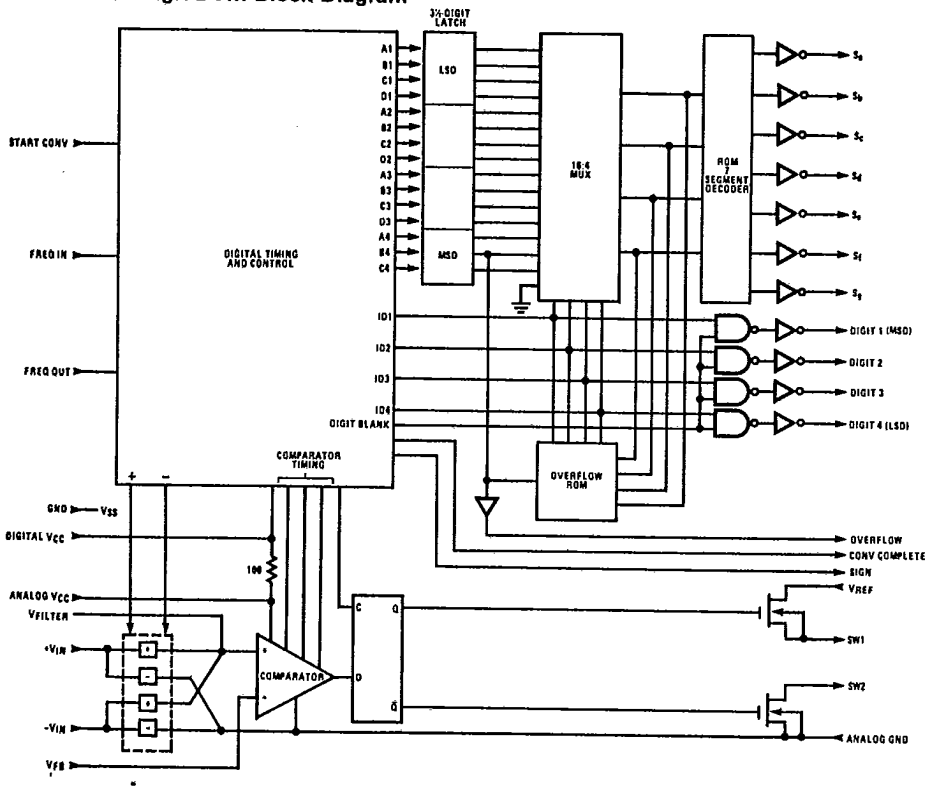
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals given for $T_A=25°C$.

Electrical Characteristics (t_c = 5 conversions/second, 0°C≤T_A≤70°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Units
Accuracy of Output Reading		V_{IN} = 0 – 2 V Full Scale V_{IN} = 0 – 200 mV Full Scale	−0.05		+0.05	% of Full Scale
Quantization Error			−1		+0	Counts
Offset Error, V_{IN} = 0 V			−0.5	+1.5	+3	mV
Rollover Error			−0.0		+0.0	mV
Analog Input Current (V_{IN}+, V_{IN}−)		T_A = 25°C	−5	±0.5	+5	nA

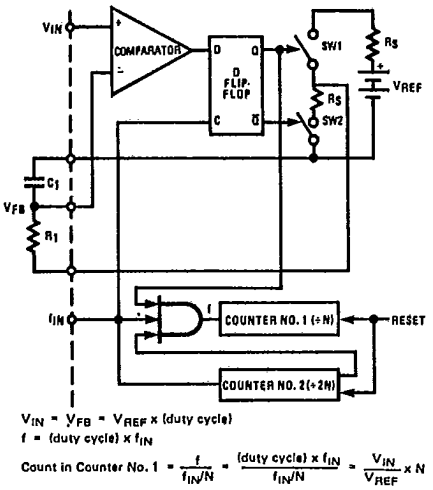
ECG2052 3½-Digit DVM Block Diagram



Theory of Operation

A schematic for the analog loop is shown in Figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level $V_{OUT} = V_{REF}$ and if Q is at a low level V_{OUT} = 0 V. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and Q outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter



An example will demonstrate this relationship. Assume the input voltage is equal to 0.500 V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000 V) and V_{FB} will charge toward 2 V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500 V and the comparator output will switch to 0 V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0 V. At this time V_{FB} will start discharging toward 0 V with a time constant R_1C_1. When V_{FB} is less than 0.5 V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0 V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\left(\frac{T_{ON}}{T_{ON}+T_{OFF}}\right) = V_{REF}\ (\text{Duty Cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}\ (\text{Duty Cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}\ (\text{Duty Cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{Duty Cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{Duty Cycle}) \times (\text{Clock})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{Count}) = \frac{f}{(\text{Clock})/N} = \frac{(\text{Duty Cycle}) \times (\text{Clock})}{(\text{Clock})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

For the ECG2052 N = 2000.

General Information

The timing diagram, shown in Figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 64,512 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ECG2052 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in Figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum times is 64,512 x $1/f_{IN}$ and the minimum time is 256 x $1/f_{IN}$.

Timing Waveforms

Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

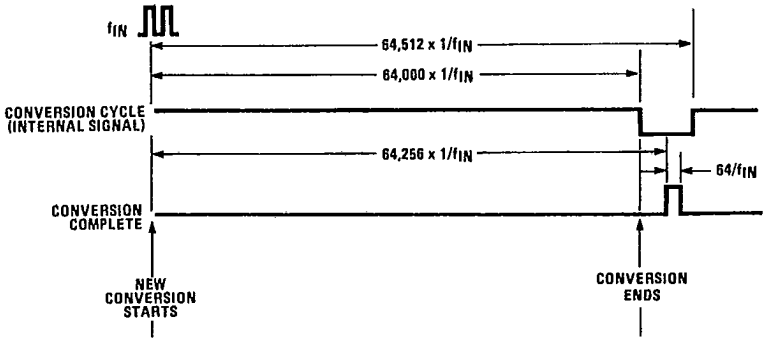
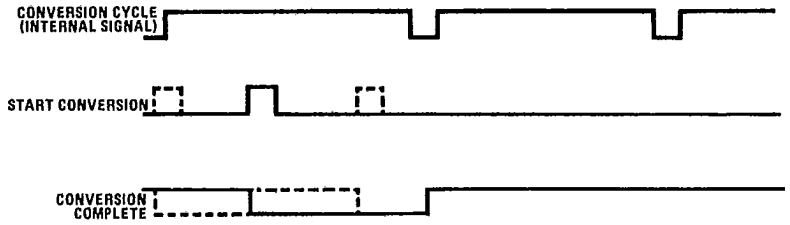


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input



Applications

System Design Considerations

Perhaps the most important thing to consider when using the ECG2052 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ECG2052 to minimize these problems but poor circuit layout can negate these features.

Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The ECG960 voltage regulator will function well and is shown in Figures 4, 5, and 6. Adding more filtering than is shown will in general increase the jitter rather than decrease it. The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DVM system which converts 0 V to 1.999 V operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or − (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in Figure 6.

Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0 nA of leakage current will cause 0.1 mV error (1.0×10^{-9}A x 100 kΩ = 0.1 mV). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.

Figure 4. 3½-Digit DVM, +1.999 Volts Full Scale

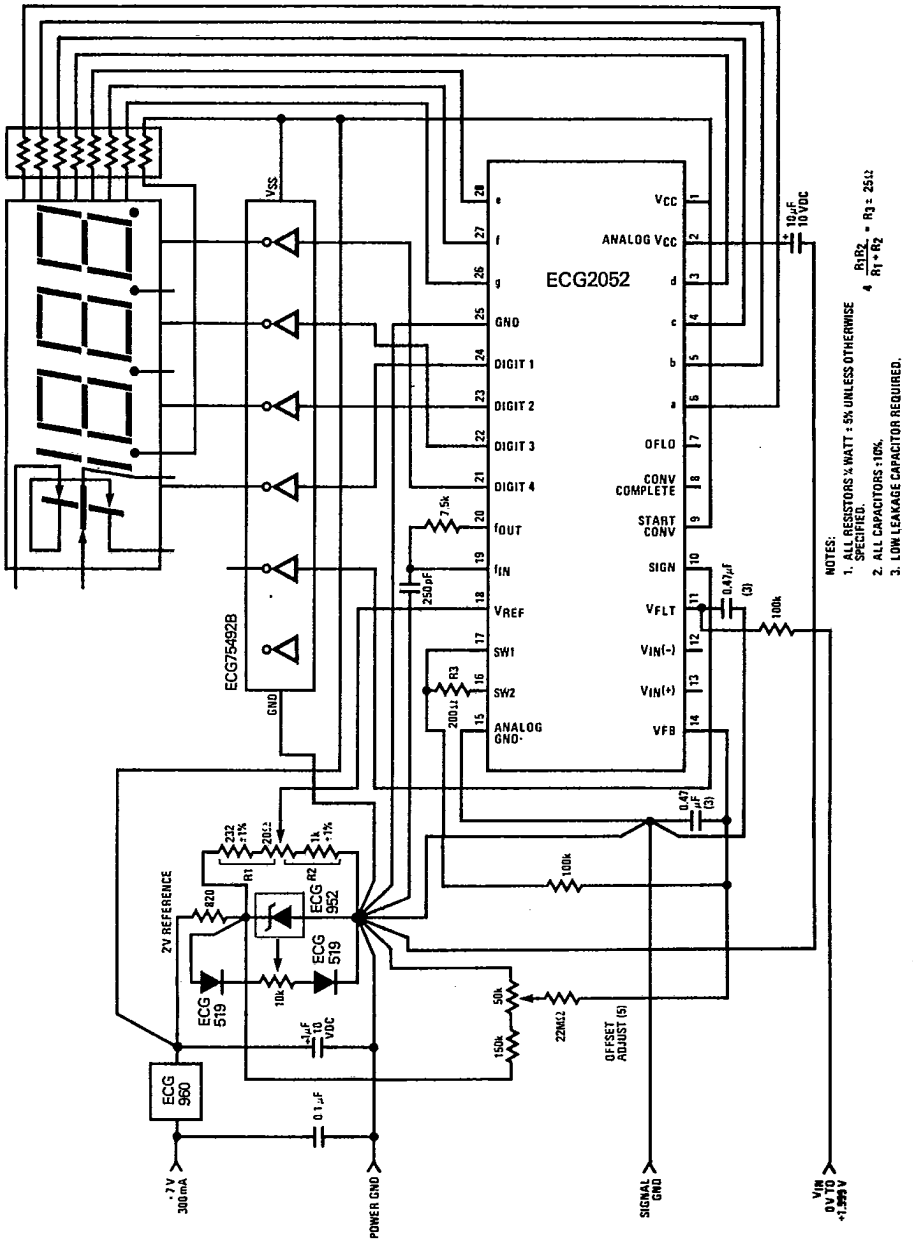


Figure 5. 3½-Digit DVM, ±1.999 Volts Full Scale

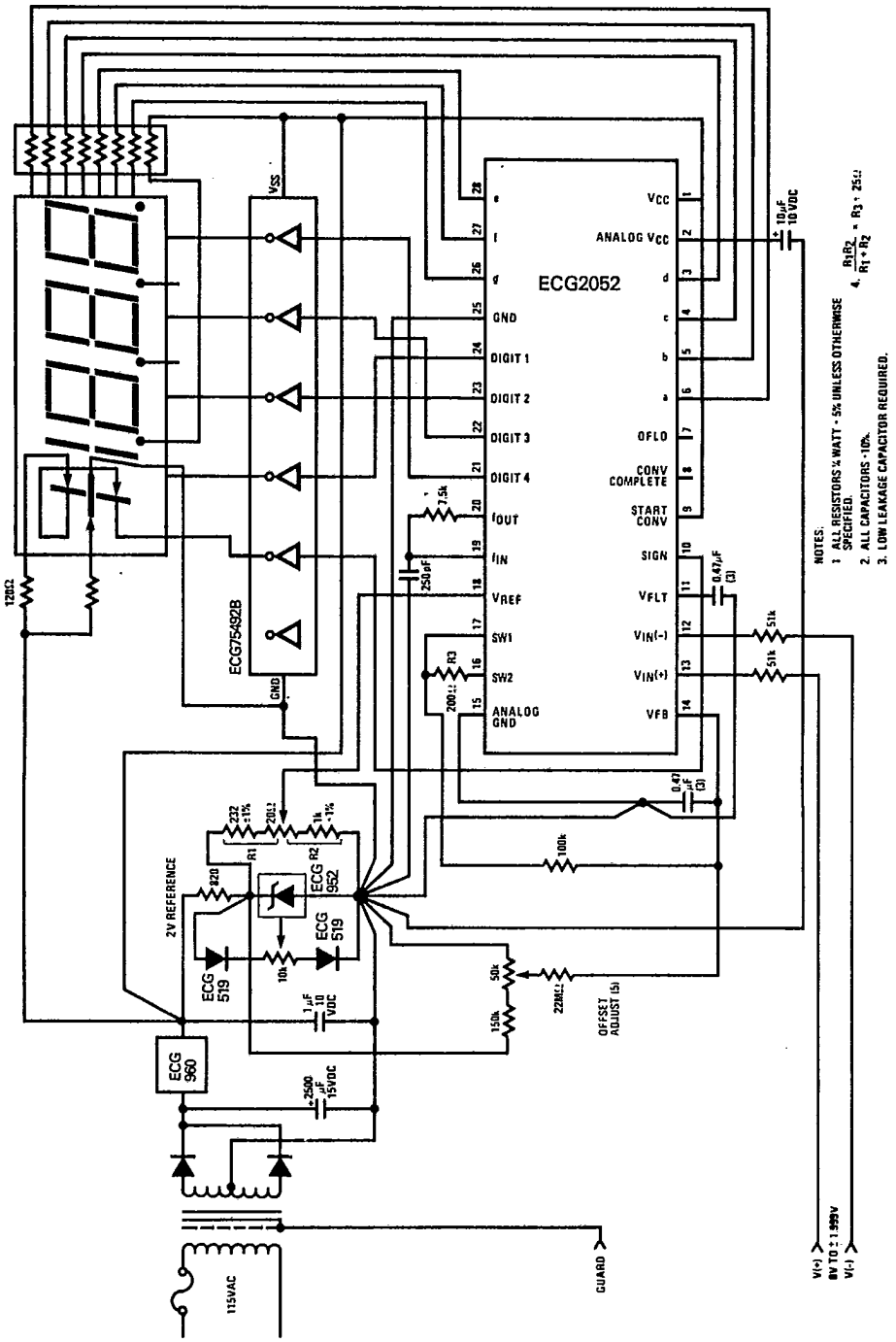


Figure 6. 3½-Digit DVM, Four Decade, ±0.2 V, ±2 V, ±20 V and ±200 V Full Scale