

ECG[®] Semiconductors

ECG833 Timing Circuit

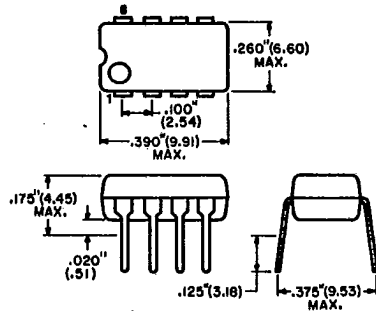
Features

- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Output can drive TTL

ECG833 is a monolithic timing circuit capable of producing accurate time delays or oscillation. ECG833 has an externally adjustable threshold level with additional terminals provided for triggering or resetting.

Typical Applications

- Time delay generation
- Sequential timing
- Linear sweep generation
- Precision timing
- Pulse generation
- Pulse shaping
- Missing pulse detection
- Pulse width modulation
- Pulse position modulation



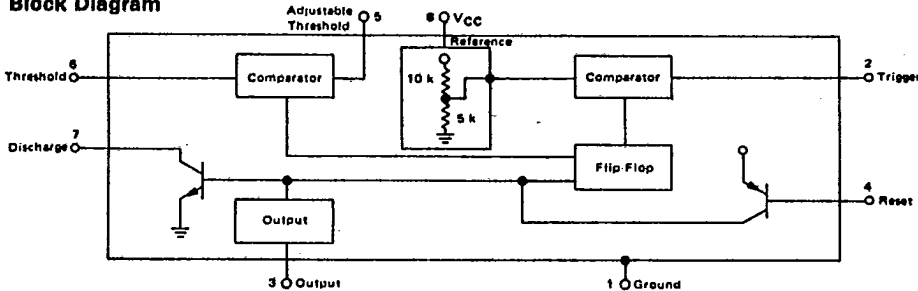
Pin Connections

1. Ground
2. Trigger
3. Output
4. Reset
5. Variable Threshold Reference
6. Threshold
7. Discharge
8. V_{cc}

Maximum Ratings (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V _{cc}	± 16	Vdc
Discharge Current (Pin 7)	I ₇	200	mA
Power Dissipation Derate above T _A = +25°C	P _D	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	T _{opg}	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

Block Diagram



87

ECG833

Electrical Characteristics ($T_A = +25^\circ\text{C}$, $V_{CC} = +5.0$ to $+14$ V unless otherwise noted.)

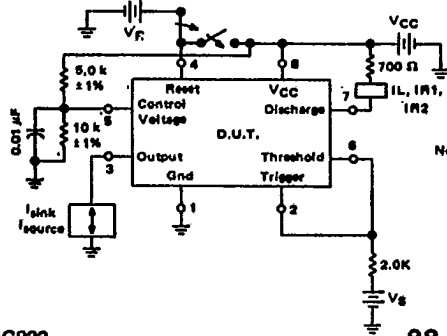
Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	--	14	V
Supply Current $V_{CC} = 5.0$ V, $R_L = \infty$ $V_{CC} = 14$ V, $R_L = \infty$ Low State (Note 1)	I_D	--	3.0 10	6.0 15	mA
Timing Error (Note 2) $R_A, R_B = 1.0$ k Ω to 100 k Ω Initial Accuracy $C = 0.1$ μF Drift with Temperature Drift with Supply Voltage		--	1.0 50 0.01	--	% PPM/ $^\circ\text{C}$ %/Volt
Threshold Voltage (Figure 2)	V_{th}	--	2/3	--	$\times V_{CC}$
Trigger Voltage $V_{CC} = 14$ V $V_{CC} = 5.0$ V	V_T	--	5.0 1.67	--	V
Trigger Current	I_T	--	0.5	--	μA
Discharge Leakage Current	I_{dis}	--	--	250	nA
Reset Current	I_R	--	0.1	--	mA
Threshold Current (Note 3)	I_{th}	--	--	1.0	μA
Output Voltage Low ($V_{CC} = 14$ V) $I_{sink} = 10$ mA $I_{sink} = 50$ mA $I_{sink} = 100$ mA $I_{sink} = 200$ mA	V_{OL}	--	0.1 0.4 2.0 2.5	0.35 1.0 3.5 --	V
Output Voltage High ($I_{source} = 25$ mA) $V_{CC} = 14$ V $V_{CC} = 5.0$ V	V_{OH}	12.75 2.75	13.3 3.3	-- --	V
Rise Time of Output	t_{OLH}	--	100	--	ns
Fall Time of Output	t_{OHL}	--	100	--	ns

Note 1: Supply current when output is high is typically 1.0 mA less.

Note 2: Tested at $V_{CC} = 5.0$ V and $V_{CC} = 14$ V.

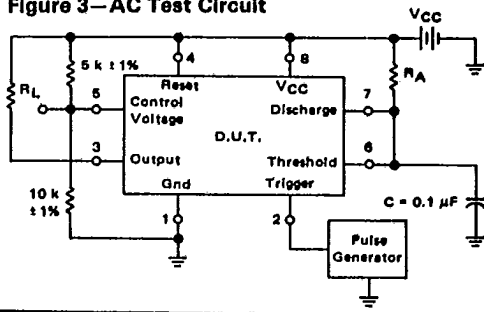
Note 3: This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total $R = 20$ megohms.

Figure 2—DC Test Circuit



Notes:
 V_{CC} = Supply Voltage: 5.0 V $< V_{CC} < 14$ V Range
 V_S = Switching Voltage: 1.4 V $< V_S < 11.0$ V Range
 When $V_S > 2/3 V_{CC}$, V_O is low ≈ 0 at $R_L = \infty$
 When $V_S < 1/3 V_{CC}$, V_O is high $\approx V_{CC}$ at $R_L = \infty$
 V_R = Reset Voltage: $V_R = 0.4$ V or 1.0 V during Reset Test
 During other tests, Pin 4 tied to V_{CC} .

Figure 3—AC Test Circuit



$R_A = 100\text{ k}$
 $t = 1.1 R_A C$ seconds

External components must be bridged so that exact values are used in the frequency formula.

TYPICAL CHARACTERISTICS
 (TA = +25°C unless otherwise noted.)

FIGURE 4 — TRIGGER PULSE WIDTH

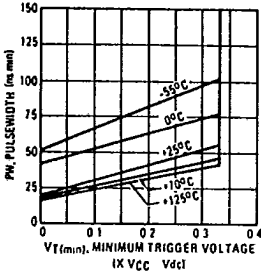


FIGURE 5 — SUPPLY CURRENT

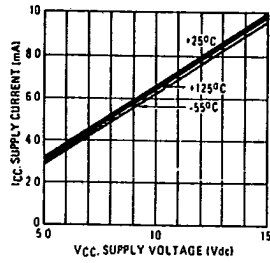


FIGURE 6 — HIGH OUTPUT VOLTAGE

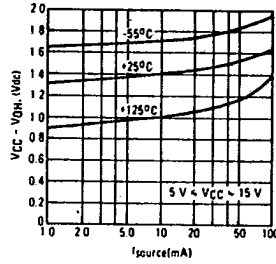


FIGURE 7 — LOW OUTPUT VOLTAGE
 @ VCC = 5.0 Vdc

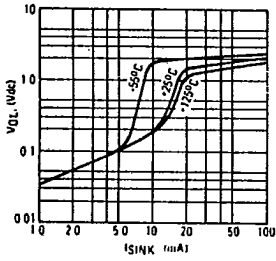


FIGURE 8 — LOW OUTPUT VOLTAGE
 @ VCC = 10 Vdc

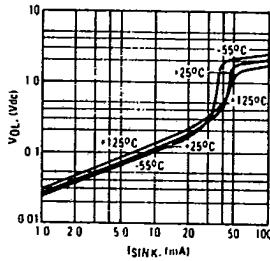


FIGURE 9 — LOW OUTPUT VOLTAGE
 @ VCC = 15 Vdc

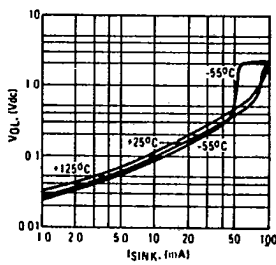


FIGURE 10 — DELAY TIME
 versus SUPPLY VOLTAGE

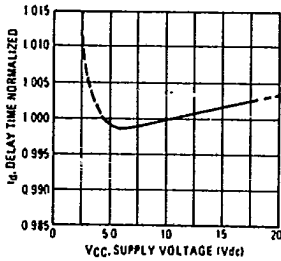


FIGURE 11 — DELAY TIME
 versus TEMPERATURE

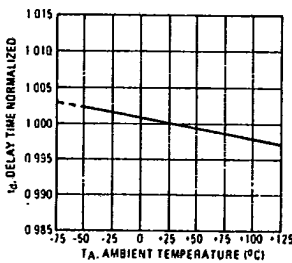


FIGURE 12 — PROPAGATION DELAY
 versus TRIGGER VOLTAGE

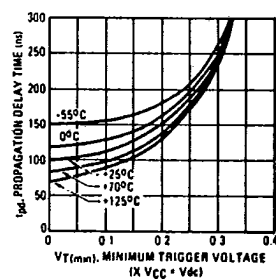


FIGURE 13 - CIRCUIT SCHEMATIC CONTROL VOLTAGE

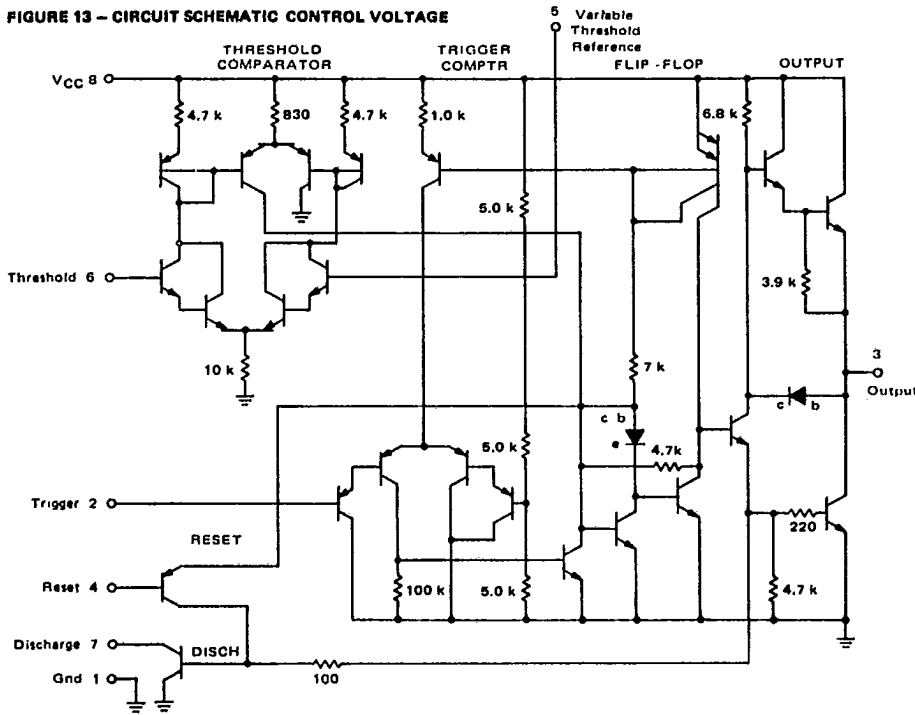
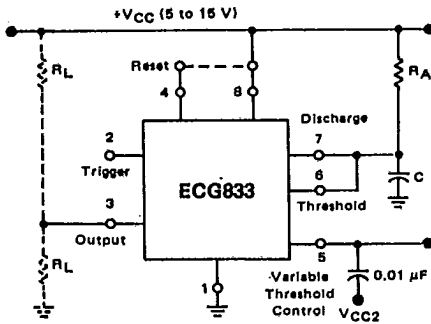


FIGURE 14 - MONOSTABLE CIRCUIT



crossing only. This cycling at zero crossing only will reduce EMI, and current surges if capacitive loads are used.

Circuit Description

In order to have exact zero crossing cycling a phase shift network (R3)(C2) is used. Diodes CR1 and CR2 limit the line voltage to V- and V+. This limited line voltage, which appears somewhat like a square wave, is used as a sync pulse when differentiated by C1 and attenuated to 1/3 by R1 and R2. Cycle time is dependent on R4 and C3. The duty cycle is set by potentiometer R4.

It should be noted that this zero crossing cycler is intended for low frequency cycling, much lower than the line frequency used.

$$T_{\text{cycle}} = 0.69 (R4)(C3) \text{ or } f_{\text{cycle}} = \frac{1.44}{(R4)(C3)}$$

Pulse Width Modulator

ECG833 is used as a pulse width modulator (PWM) with the ECG955M being utilized as an astable. The ECG833 can be used as an astable in place of the ECG955M if an external reference of approximately 2/3 VCC is used at Pin 5.

Applications Information

The ECG833 can be used in any application where the ECG955M is currently being used as long as an external reference is supplied. The applications listed below are unique to the ECG833.

Zero Crossing Cycler

This circuit (see Figure 15) is most useful where it is necessary to cycle a thyristor at some frequency and duty cycle at line zero

FIGURE 15 - ZERO CROSSING CYCLER

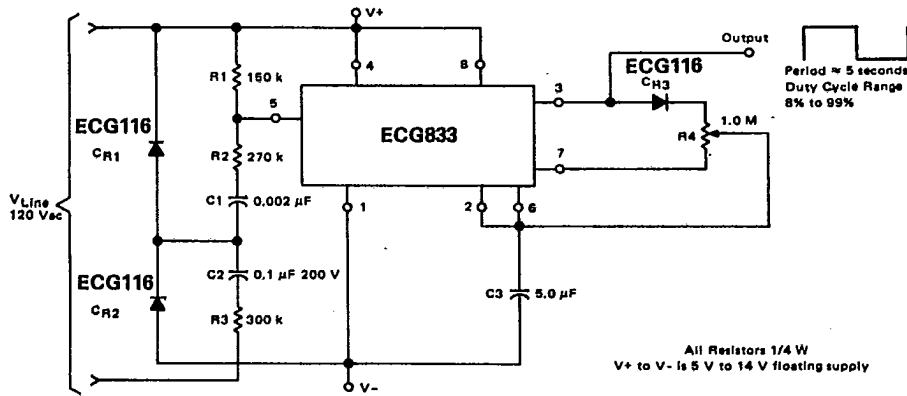
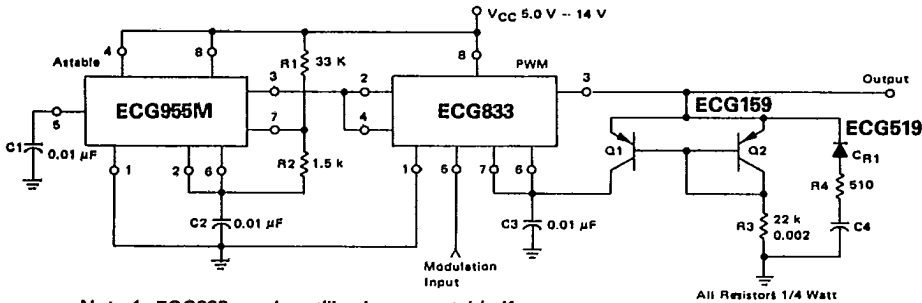


FIGURE 16 - PULSE WIDTH MODULATOR



Note 1. ECG833 can be utilized as an astable if an external 2/3 ratio resistive divider is used at pin 5.

Note 2. See waveforms.

The transistors Q1 and Q2 are configured as a current mirror to provide a linear voltage ramp across C3. This constant current scheme attributes a relatively linear transfer characteristics for the pulse width modulator. Several considerations must be made when using this circuit.

1. The minimum duty cycle out is limited to the complement of the input signal. (i.e., a 95% duty cycle astable driving the PWM will give a minimum duty cycle output of ≈5%.)

The maximum duty cycle out will also be limited to the maximum duty cycle in.

2. For the astable frequency:

$$f = 1/T = \frac{1.44}{(R_1 + 2R_2)C}$$

3. Duty cycle (D.C.) for the astable:

$$DC = \frac{R_2}{R_1 + 2R_2}$$

For best results the charge time of C3 in the pulse width modulator should be equal to the period of the astable.

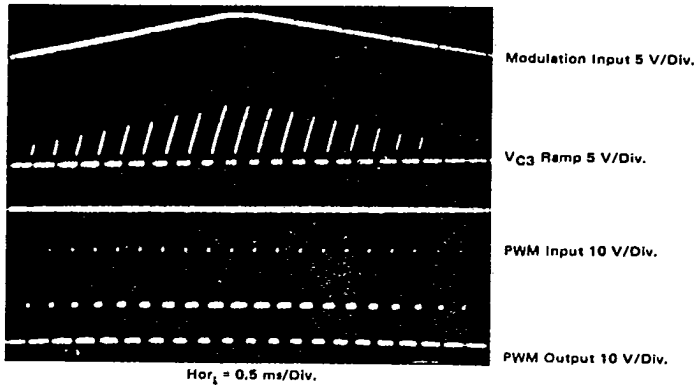
$$\frac{I_{Q1}}{C3(V_{CC}-1)} = f_{in} = \frac{1}{T_{C3}} I_{Q1} \cong I_{Q2} = \frac{V_{CC}-V_{BE}}{R_3}$$

V_{CC} = 10 V linearity typically 3% modulation input from 2 volts to 8 volts.

Voltage Controlled Oscillator

The VCO circuit, which has a nonlinear transfer characteristic will operate satisfactorily up to 200 kHz. The VCO input range is ef-

FIGURE 17 - PULSE WIDTH MODULATOR WAVEFORMS



fective from $1/3 V_{cc}$ to $V_{cc} - 2 V$, with the highest control voltage producing the lowest output frequency. The equation for the frequency is:

$$f_{out} \cong \frac{1}{\ln \left(1 - \frac{V_5 - 1/3 V_{cc}}{2/3 V_{cc}} \right) (R_1 + R_2)C_1 + \ln \left(\frac{V_5 - 1/3 V_{cc}}{V_5} \right) R_2C_1}$$

$V_5 =$ VCO input control voltage

It should be noted that, the output duty cycle will vary somewhat over the VCO input control range.

Comparator with Time Out

ECG833 is used as a comparator with the capability of a timing output pulse when the Inverting input (Pin 6) is \geq the non-inverting input (Pin 5). The frequency of the pulses for the values of R2 and C1 as shown in Figure 19 is approximately 2.0 Hz, and the pulse width 0.3 ms, $f_p =$ frequency of pulses while Pin 6 voltage is above voltage at Pin 5.

The function of R1 is to limit di/dt, when charging C1.

$$f_p \cong \frac{1}{R_2C_1} \text{ or } T_p \cong R_2C_1$$

Schmitt Trigger

The ECG833 is very useful as a Schmitt Trigger as shown in Figure 20. The lower trigger point is fixed at $1/3 V_{cc}$, but the upper trigger point is adjustable by means of Pin 5 from $1/3 V_{cc}$ to slightly less than V_{cc} . The schmitt trigger will operate with input frequencies up to 50 kHz.

Figure 18

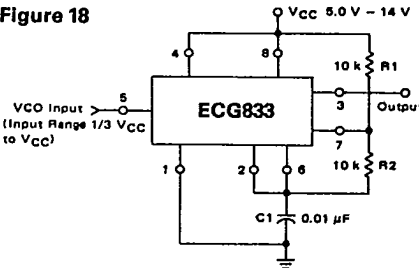


Figure 19

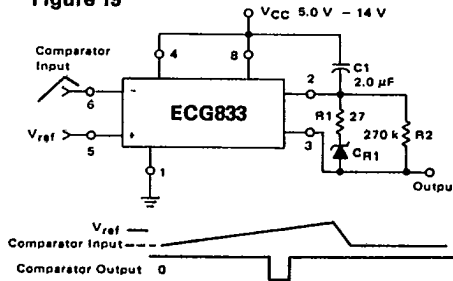


Figure 20

