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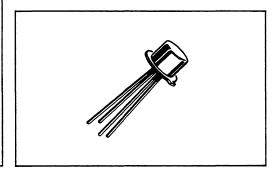
3N128

SILICON N-CHANNEL MOS FIELD-EFFECT TRANSISTOR

 \ldots designed for VHF amplifier and oscillator applications in communications equipment.

- High Forward Transadmittance –
 |yfs| = 5000 μmhos (Min) @ f = 1.0 kHz
- Low Input Capacitance –
 C_{iss} = 7.0 pF (Max) @ f = 1.0 MHz
- Low Noise Figure –
 NF = 5.0 dB (Max) @ f = 200 MHz
- High Power Gain —
 PG = 13.5 dB (Min) @ f = 200 MHz
- Complete "y" Parameter Curves
- Third Order Intermodulation Distortion Performance Curve Provided

N-CHANNEL MOS FIELD-EFFECT TRANSISTOR



* MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	+20	Vdc
Drain-Gate Voltage	V _{DG}	+20	Vdc
Gate-Source Voltage	V _{GS}	±10	Vdc
Drain Current	ID	50	mAdc
Power Dissipation @ T _A = 25 ^o C Derate above 25 ^o C	PD	330 2.2	mW mW/ ^O C
Operating and Storage Junction Temperature Range	T _J ,T _{stg}	-65 to +175	°C

^{*}Indicates JEDEC Registered Data.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	5.31	5.84	0.209	0.230	
В	4.52	4.95	0.178	0.195	
C	4.32	5.33	0.170	0.210	
D	0.41	0.53	0.016	0.021	
E	_	0.76	-	0.030	
F	0.41	0.48	0.016	0.019	
G	2.54 BSC		0.100 BSC		
Н	0.91	1.17	0.036	0.046	
J	0.71	1.22	0.028	0.048	
K	12.70	-	0.500	-	
L	6.35	_	0.250	_	
M	45°BSC		45° BSC		
N	1.27 BSC		0.050 BSC		
P	_	1.27	_	0.050	

CASE 20-03 TO-206AF (TO-72)

HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while handling, testing, or in actual operation, by following the procedures outlined below:

- To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
- Avoid unnecessary handling. Pick up devices by the case instead of the leads.
- Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				·
Gate-Source Breakdown Voltage (1) $(I_G = -10 \mu\text{Adc}, V_{DS} = 0)$	V(BR)GSS	-50	_	Vdc
Gate-Source Cutoff Voltage (V _{DS} = 15 Vdc, I _D = 50 μAdc)	V _{GS(off)}	-0.5	-8.0	Vdc
Gate Reverse Current $(V_{GS} = -8.0 \text{ Vdc}, V_{DS} = 0)$ $(V_{GS} = -8.0 \text{ Vdc}, V_{DS} = 0, T_A = 125^{\circ}\text{C})$	¹ GSS		0.05 5.0	nAdc
ON CHARACTERISTICS				
Zero-Gate-Voltage Drain Current (2) $(V_{DS} = 15 \text{ Vdc}, V_{GS} = 0)$	IDSS	5.0	25	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transadmittance $(V_{DS} = 15 \text{ Vdc}, I_D = 5.0 \text{ mAdc}, f = 1.0 \text{ kHz})$	Vfs	5000	12,000	μmhos
Forward Transconductance $(V_{DS} = 15 \text{ Vdc}, I_D = 5.0 \text{ mAdc}, f = 200 \text{ MHz})$	Re(y _{fs})	5000	_	μmhos
Output Conductance (V _{DS} = 15 Vdc, I _D = 5.0 mAdc, f = 200 MHz)	Re(yos)		500	μmhos
Input Conductance (V _{DS} = 15 Vdc, I _D = 5.0 mAdc, f = 200 MHz)	Re(y _{is})		800	μmhos
Input Capacitance (V _{DS} = 15 Vdc, I _D = 5.0 mAdc, f = 1.0 MHz)	C _{iss}	_	7.0	pF
Reverse Transfer Capacitance (V _{DS} = 15 Vdc, I _D = 5.0 mAdc, f = 1.0 MHz)	C _{rss}	0.05	0.35	pF
Noise Figure $(V_{DS} = 15 \text{ Vdc}, I_D = 5.0 \text{ mAdc}, f = 200 \text{ MHz})$	NF		5.0	dB
Power Gain (V _{DS} = 15 Vdc, I _D = 5.0 mAdc, f = 200 MHz)	PG	13.5	23	dB

*Indicates JEDEC Registered Data.

- (1) Caution Destructive Test, can damage gate oxide beyond operation.
- (2) Pulse Test: Pulse Width = 300 μ s, Duty Cycle = 2.0%.

TYPICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C)$

FIGURE 1 - DRAIN CHARACTERISTICS

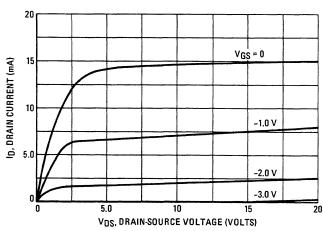
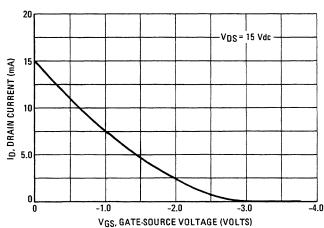


FIGURE 2 - TRANSFER CHARACTERISTICS





MOTOROLA Semiconductor Products Inc.

TYPICAL 1 kHz DRAIN CHARACTERISTICS

 $(T_A = 25^{\circ}C, V_{DS} = 15 \text{ Vdc}, f = 1.0 \text{ kHz})$

FIGURE 3 – FORWARD TRANSADMITTANCE versus GATE BIAS VOLTAGE

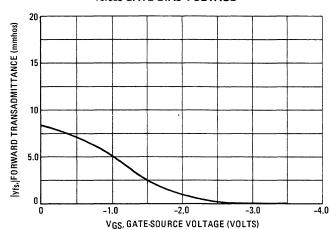
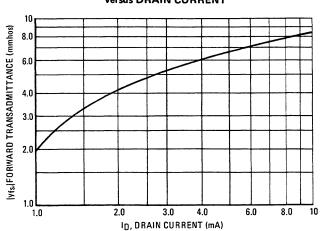


FIGURE 4 — FORWARD TRANSADMITTANCE versus DRAIN CURRENT



TYPICAL 200 MHz COMMON-SOURCE ADMITTANCE CHARACTERISTICS

 $(T_A = 25^{\circ}C, V_{DS} = 15 \text{ Vdc}, f = 200 \text{ MHz})$

FIGURE 5 - INPUT ADMITTANCE (yis) COMPONENTS

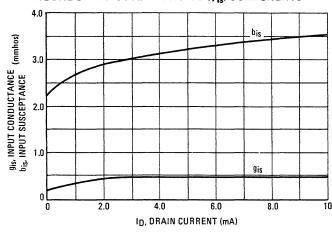


FIGURE 6 - FORWARD TRANSADMITTANCE (yfs) COMPONENTS

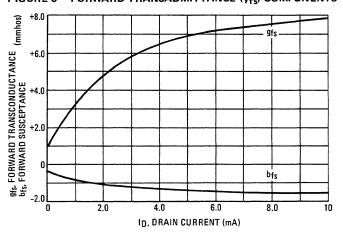


FIGURE 7 - REVERSE TRANSADMITTANCE (yrs) COMPONENTS

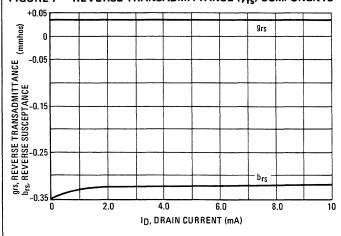


FIGURE 8 – OUTPUT ADMITTANCE (yos) COMPONENTS

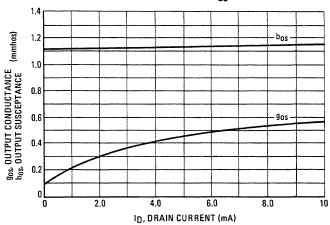




FIGURE 9 – POWER GAIN AND NOISE FIGURE versus DRAIN CURRENT

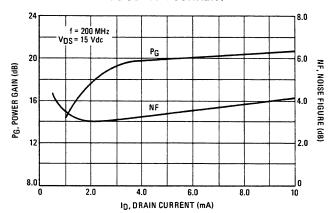


FIGURE 10 – POWER GAIN AND NOISE FIGURE versus DRAIN VOLTAGE

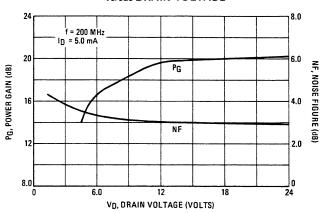


FIGURE 11 - THIRD ORDER INTERMODULATION DISTORTION

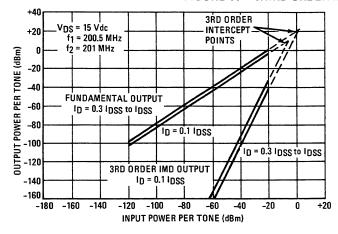
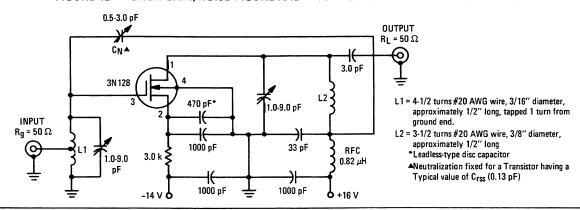


Figure 11 shows the typical third order intermodulation distortion (IMD) performance of the 3N128 at 200 MHz.

Both fundamental output and third order IMD output characteristics are plotted. The curves have been extrapolated to show the third order intermodulation output intercept point.

Performance for drain currents from I_{DSS} to 0.1 I_{DSS} , is given. The power gain and noise figure test amplifier shown in Figure 12 was used to generate the IMD data.

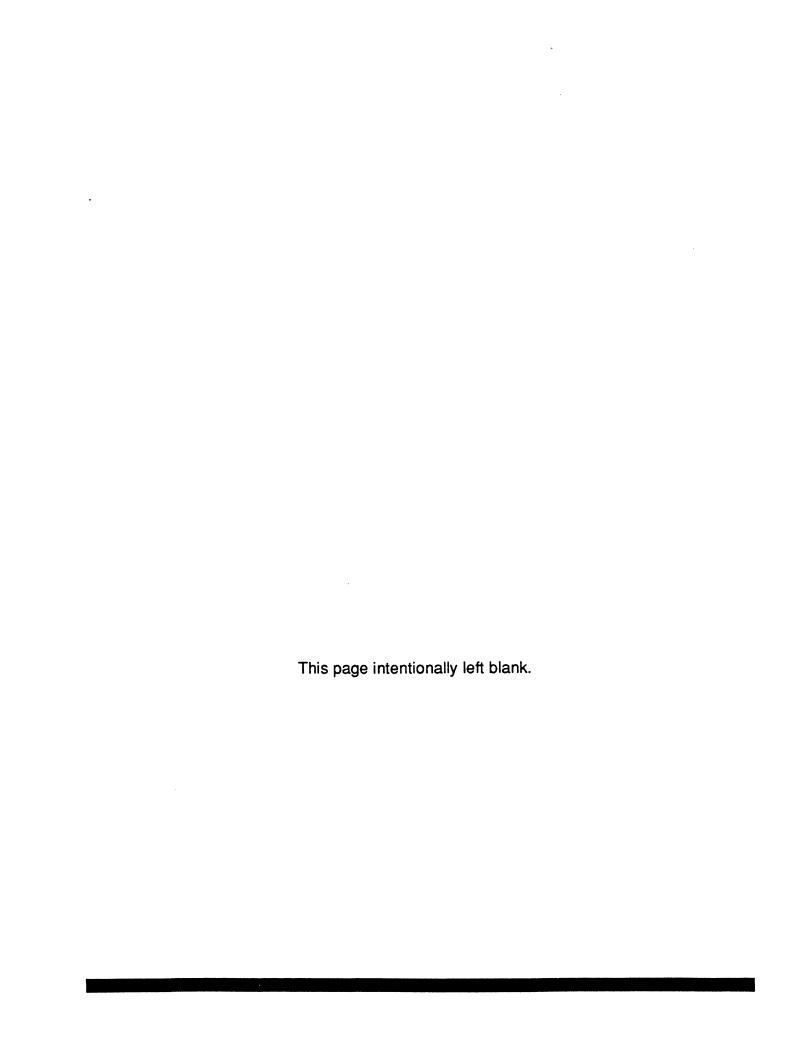
FIGURE 12 - POWER GAIN, NOISE FIGURE AND INTERMODULATION DISTORTION TEST CIRCUIT

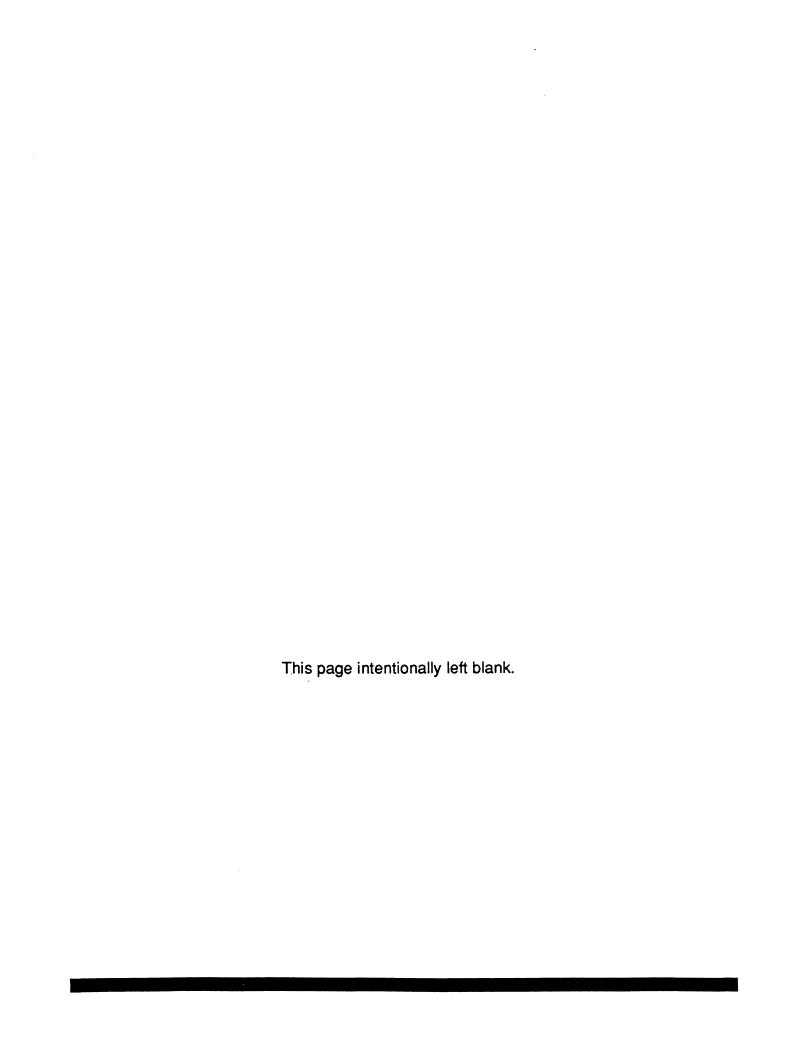


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