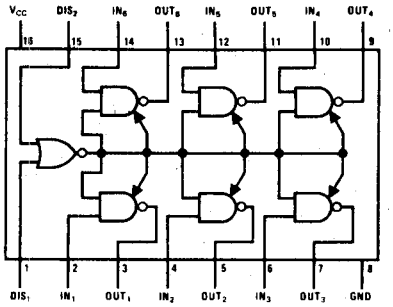
TTL Logic Diagrams (cont'd)

Diag. 239 — 16-Pin DIP See Fig. D8

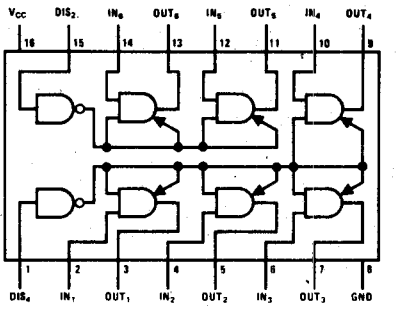
ECG80C96



Hex Inverter/Buffer with 3-State Output (Common Enable)

Diag. 240 — 16-Pin DIP See Fig. D8

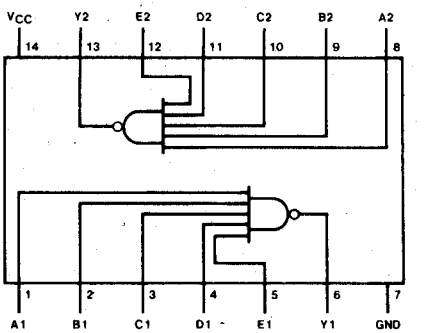
ECG80C97



Hex Buffer with 3-State Output (2-Line/4-Line Enable)

Diag. 241 — 14-Pin DIP See Fig. D6

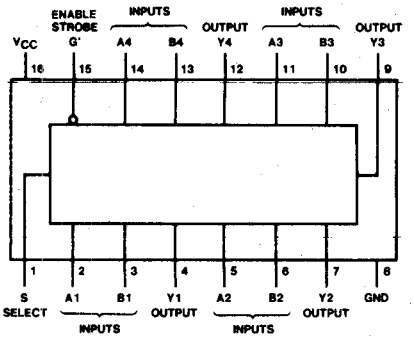
ECG8092



Dual 5-Input NAND Gate

Diag. 242 — 16-Pin DIP See Fig. D8

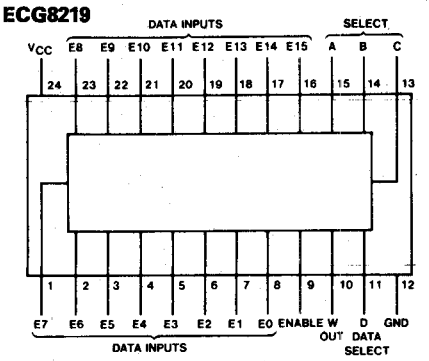
ECG8123



Quad 2-Line-to-1-Line Data Selector/Multiplexer with 3-state Output

Diag. 243 — 24-Pin DIP See Fig. D15

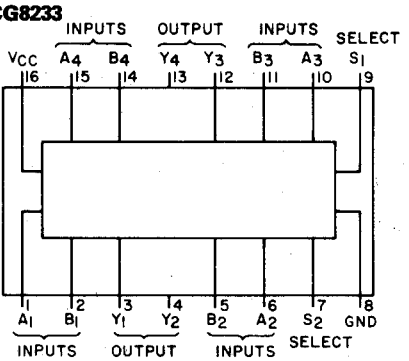
ECG8219



16-Line-to-1-Line Data Selector/Multiplexer with Inverting 3-State Output

Diag. 244 — 16-Pin DIP See Fig. D8

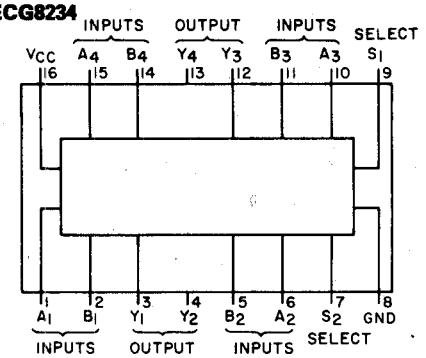
ECG8233



Quad 2-Line-to-1-Line Data Selector/Multiplexer

Diag. 245 — 16-Pin DIP See Fig. D8

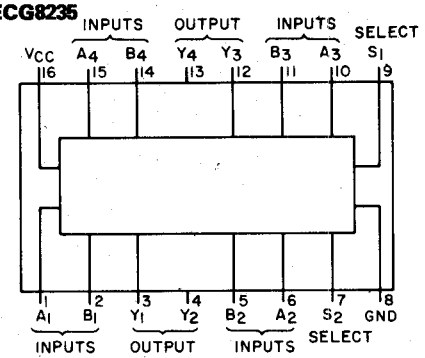
ECG8234



Quad 2-Line-to-1-Line Data Selector/Multiplexer with Inverting Output

Diag. 246 — 16-Pin DIP See Fig. D8

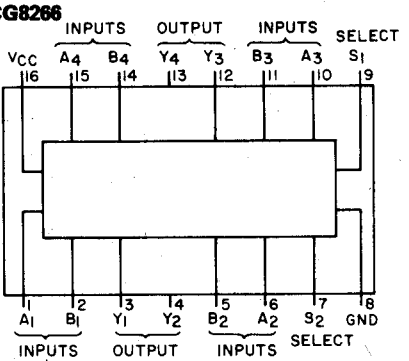
ECG8235



Quad 2-Line-to-1-Line Data Selector/Multiplexer with Open Collector Output

Diag. 247 — 16-Pin DIP See Fig. D8

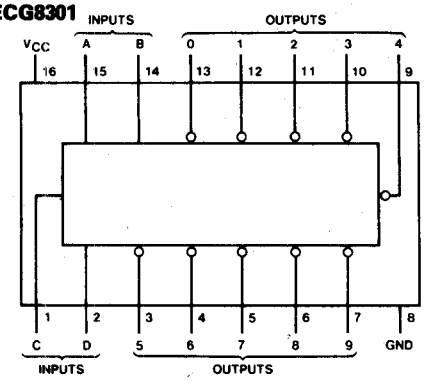
ECG8266



Quad 2-Line-to-1-Line Data Selector/Multiplexer with Conditional Outputs

Diag. 248 — 16-Pin DIP See Fig. D8

ECG8301

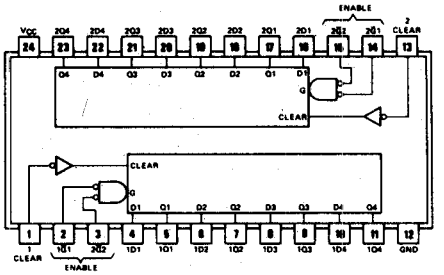


BCD-to-Decimal Decoder

Diag. 249 — 24-Pin DIP See Fig. D15

(See Also Diag. 269)

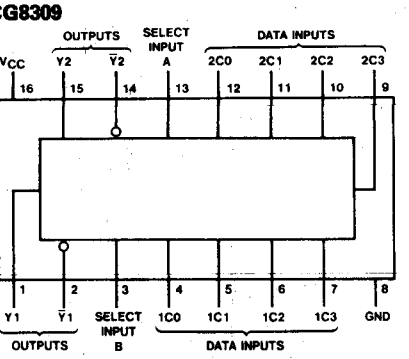
ECG8308



Dual 4-Bit Latch

Diag. 250 — 16-Pin DIP See Fig. D8

ECG8309



Dual 4-Line-to-1-Line Data Selector/Multiplexer with Complementary Output

Package Outlines - See Page 1-357