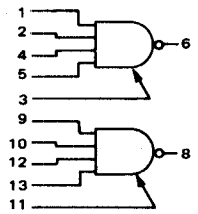
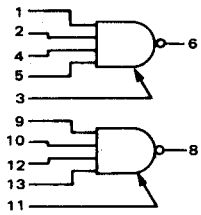
HTL High Threshold Logic

ECG9660 14-Pin DIP See Fig. D6
Expandable Dual 4-Input NAND Gate (Active Pull-Up), V_{CC} = +15 V (Nom.)



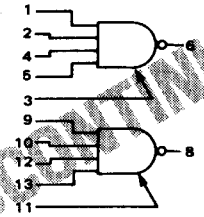
V_{CC} = Pin 14, GND = Pin 7

ECG9661 14-Pin DIP See Fig. D6
Expandable 4-Input NAND Gate (Passive Pull-Up), V_{CC} = +15 V (Nom.)



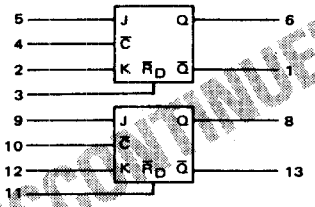
V_{CC} = Pin 14, GND = Pin 7

ECG9662 14-Pin DIP See Fig. D6
Expandable 4-Input Line NAND Driver (Active Pull-Up), V_{CC} = +15 V (Nom.)



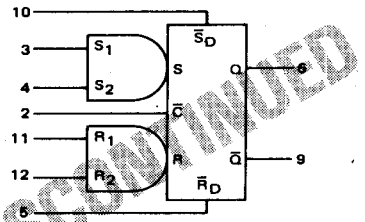
V_{CC} = Pin 14, GND = Pin 7

ECG9663 14-Pin DIP See Fig. D6
Dual J-K Flip-Flop, V_{CC} = +15 V (Nom.)



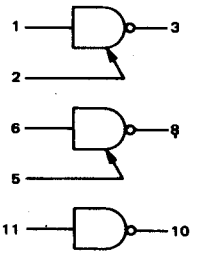
V_{CC} = Pin 14, GND = Pin 7

ECG9664 14-Pin DIP See Fig. D6
M/S R-S Flip-Flop, V_{CC} = +15 V (Nom.)



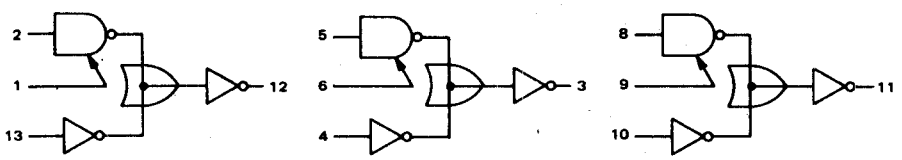
V_{CC} = Pin 14, GND = Pin 7

ECG9665 14-Pin DIP See Fig. D6
Triple Level Translator tp = 40 ns Typ, V_{CC} = +15 V (Nom.)



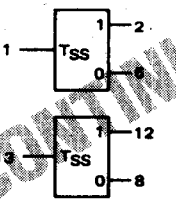
V_{CC} = Pin 14, GND = Pin 7

ECG9666 14-Pin DIP See Fig. D6
Triple Level Translator tp = 75 ns Typ, V_{CC} = +15 V (Nom.)



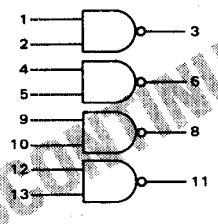
V_{CC} = Pin 14, GND = Pin 7

ECG9667 14-Pin DIP See Fig. D6
Dual Monostable Multivibrator, V_{CC} = +15 V (Nom.)



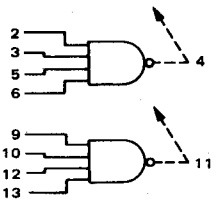
V_{CC} = Pin 14, GND = Pin 7

ECG9668 14-Pin DIP See Fig. D6
Quad 2-Input NAND Gate (Passive Pull-Up), V_{CC} = +15 V (Nom.)



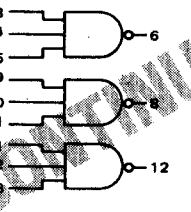
V_{CC} = Pin 14, GND = Pin 7

ECG9669 14-Pin DIP See Fig. D6
Dual 4-Input Expander, V_{CC} = +15 V (Nom.)



V_{CC} = Pin 14, GND = Pin 7

ECG9670 14-Pin DIP See Fig. D6
Triple 3-Input NAND Gate (Passive Pull-Up), V_{CC} = +15 V (Nom.)



V_{CC} = Pin 14, GND = Pin 7

Package Outlines - See Page 1-357