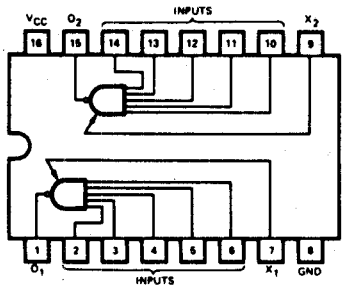
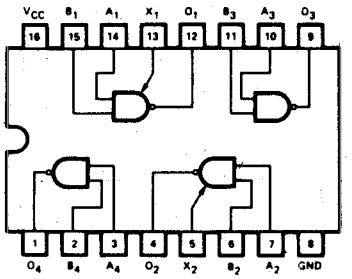
HLL High Level Logic Circuits

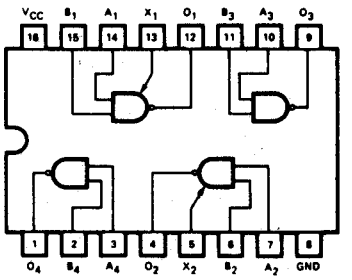
ECG9301 16-Pin DIP See Fig. D8
Dual 5-Input Power NAND Gate (Active Pull-Up), V_{CC} = +15 V (Nom.)



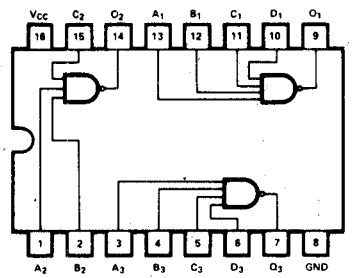
ECG9302 16-Pin DIP See Fig. D8
Quad 2-Input NAND Buffer Gate (Open Collector), V_{CC} = +15 V (Nom.)



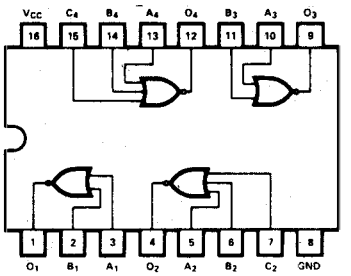
ECG9303 16-Pin DIP See Fig. D8
Quad 2-Input NAND Buffer Gate (Passive Pull-Up), V_{CC} = +15 V (Nom.)



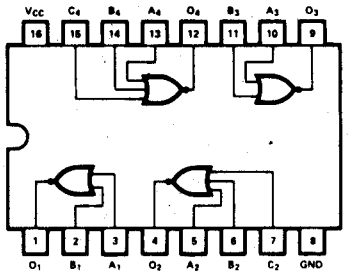
ECG9304 16-Pin DIP See Fig. D8
Triple 4,3,4 Input NAND Gate (Passive Pull-Up), V_{CC} = +15 V (Nom.)



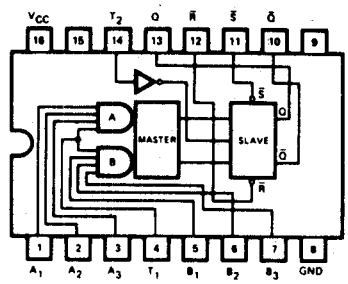
ECG9306 16-Pin DIP See Fig. D8
2,2,3,3 Input NOR Gate (Active Pull-Up), V_{CC} = +15 V (Nom.)



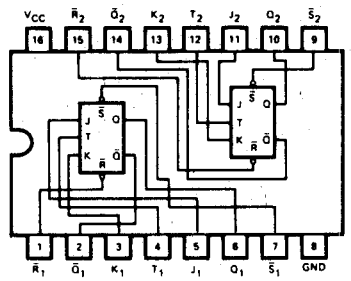
ECG9307 16-Pin DIP See Fig. D8
2,2,3,3 Input NOR Gate (Open Collector), V_{CC} = +15 V (Nom.)



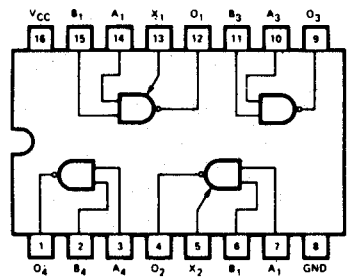
ECG9311 16-Pin DIP See Fig. D8
Master/Slave Flip-Flop (Active Pull-Up), V_{CC} = +15 V (Nom.)



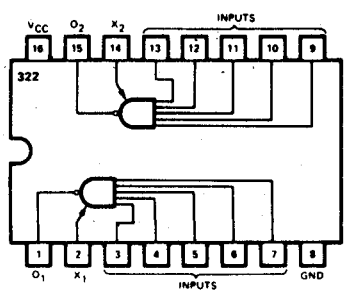
ECG9312 16-Pin DIP See Fig. D8
Dual J-K Flip-Flop (Active Pull-Up), V_{CC} = +15 V (Nom.)



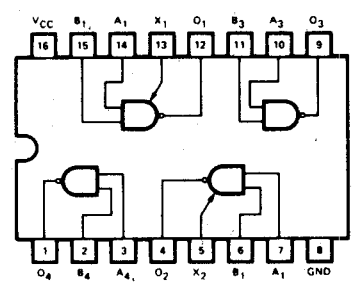
ECG9321 16-Pin DIP See Fig. D8
Qual 2-Input NAND Gate (Active Pull-Up), V_{CC} = +15 V (Nom.)



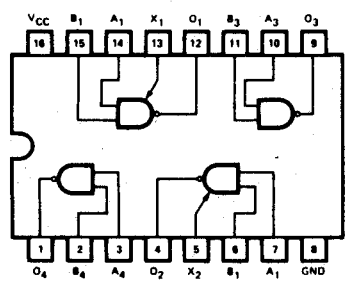
ECG9322 16-Pin DIP See Fig. D8
Dual 5-Input NAND Gate (Active Pull-Up), V_{CC} = +15 V (Nom.)



ECG9323 16-Pin DIP See Fig. D8
Quad 2-Input NAND Gate (Open Collector), V_{CC} = +15 V (Nom.)



ECG9324 16-Pin DIP See Fig. D8
Quad 2-Input NAND Gate (Passive Pull-Up), V_{CC} = +15 V (Nom.)



Package Outlines - See Page 1-357