

# Linear IC and Module Circuits (cont'd)

**ECG7111** 52-Pin DIP See Fig. L126C  
Single Chip TV Signal Processor,  
 $V_{cc1} = 12\text{ V}$ ,  $V_{cc2} = 9\text{ V}$

VERTICAL GND	1	52	COMPOSITE VID IN 1H DELAY
BLACK LEVEL DET FIL	2	51	PICTURE ADJ
COMPOSITE VID IN	3	50	Y/C SEP OUT 2 C
HORIZ SYNC SEP IN	4	49	CONTRAST CTRL
VERT SYNC SEP IN	5	48	Y/C SEP OUT 1 Y
VERT OUT	6	47	Y CLAMP CAP
VERT SAWTOOTH WAVE CAP	7	46	VID SIG IN
VERT FEEDBACK IN	8	45	DC REGEN ADJ
VERT PULSE OUT	9	44	BRIGHTNESS CTRL
VERT FIL	10	43	DELAY TIME ADJ
VERT SYNC SEP IN	11	42	CHROMA SIG IN
HOLD DOWN IN	12	41	ACC DET FIL
HORIZ AFC FIL	13	40	CLR CTRL
HOLD DOWN REF VOLT	14	39	BLACK LEVEL START POINT ADJ
PHASE COMP FBP IN	15	38	WHITE PK LIM ADJ
SYNC DET FIL	16	37	TINT CTRL
503 KHz OSC	17	36	VCC 2
HORIZ VCC	18	35	VCC 1
HORIZ BLANK PULSE IN	19	34	3.58 MHz OSC
GND	20	33	GND
HORIZ DRVR PULSE OUT	21	32	FLESH CLR PHASE ADJ
SHUT DOWN IN	22	31	AIC FIL FLESH CLR COMP ON/OFF R IN
Y OUT	23	30	G IN
B-Y OUT	24	29	B IN
G-Y OUT	25	28	B IN
R-Y OUT	26	27	Ys IN

**ECG7112** 18-Pin DIP See Fig. L115  
Video/Chroma Signal Processor,  
 $V_{cc} = 12\text{ V Typ}$

Y SIGNAL INPUT	1	18	CONTRAST CTRL
PICTURE CTRL	2	17	VCC
Y CLAMP CAP	3	16	COLOR CTRL
BRIGHT CTRL	4	15	R-Y INPUT
PED CLAMP INPUT	5	14	R-Y CLAMP CAP
BLANKING INPUT	6	13	G-Y CLAMP CAP
R OUTPUT	7	12	B-Y INPUT
G OUTPUT	8	11	B-Y CLAMP CAP
B OUTPUT	9	10	GROUND

**ECG7113** 16-Pin SIP-HS See Fig. L175  
Dual BTL AF PO, 14 W,  $V_{cc} = 13.2\text{ V}$ ,  $R_L = 4\ \Omega$

VCC	1
OUTPUT 1	2
GROUND 1	3
OUTPUT 1	4
STAND-BY MODE (OV)	5
INPUT 1	6
NFB 1	7
NFB 1	8
NFB 2	9
GROUND (INPUT)	10
NFB 2	11
INPUT 2	12
RIPPLE FILTER	13
OUTPUT 2	14
GROUND 2	15
OUTPUT 2	16

**ECG7114** 17-Pin SIP See Fig. L173  
Quad AF PO 11 W/Ch, 2 x 22 W (BTL),  
 $V_{cc} = 14\text{ V}$ ,  $R_L = 2\ \Omega$

NON-INV INPUT 1	1
INV INPUT 1	2
GROUND (SIGNAL)	3
RIPPLE REJ FIL	4
VCC	5
OUTPUT 1	6
GROUND	7
OUTPUT 2	8
NC	9
OUTPUT 3	10
GROUND	11
OUTPUT 4	12
VCC	13
MUTE/STANDBY SW	14
NC	15
INV INPUT 2	16
NON INV INPUT 2	17

**ECG7115** 18-Pin DIP See Fig. L115  
Horizontal/Vertical Signal Processor,  
 $V_{cc} = 12\text{ V Typ}$

LINE FLYBACK CONTROL	1	18	TIME CONSTANT
FLYBACK IN	2	17	PHASE COMPARE
PHASE COMPARE	3	16	HORIZ OSC
HORIZ OUT PULSE	4	15	VCC
GROUND	5	14	HORIZ OSC
BURST GATE BLANKING OUT	6	13	COINCIDENCE DET
MUTE OUT	7	12	TV TRANS ID
PROTECT IN	8	11	COMPOSITE VIDEO IN
VERT/COMPOSITE SYNC OUT	9	10	COMPOSITE SYNC GEN

**ECG7116** 20-Pin DIP See Fig. L118A  
PLL Stereo Decoder,  $V_{cc} = 8.5\text{ V Typ}$

MULTIPLEXER IN	1	20	GROUND
PILOT DETECTOR	2	19	PHASE DETECTOR
LED DRIVER OUT	3	18	L-R DE-EMPHASIS
VCO	4	17	L-R DE-EMPHASIS
VCC	5	16	SMOOTH MONO STEREO CONTROL
SOURCE SEL IN	6	15	VO DECODER LEFT DE-EMPHASIS
MUTE IN	7	14	VO DECODER RIGHT DE-EMPHASIS
IN 2 LEFT	8	13	IN 1 LEFT
IN 2 RIGHT	9	12	IN 1 RIGHT
VO RIGHT	10	11	VO LEFT

Package Outlines - See Page 1-269

